OPTIMIZATION OF SIGE HBT BICMOS ANALOG BUILDING BLOCKS FOR OPERATION IN EXTREME ENVIRONMENTS

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OPTIMIZATION OF SIGE HBT BICMOS ANALOG BUILDING BLOCKS FOR OPERATION IN EXTREME ENVIRONMENTS

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SUMMARY

The objective of this research is to optimize SiGe HBT BiCMOS analog building blocks for operation in extreme environments. A single-event transient (SET) is defined as a change of state due to a single ionizing particle (e.g., ion, electron, and photon) striking a sensitive node of a microelectronic device such as an operational amplifier, semiconductor memory, or microprocessor. This perturbation can cause an error in device operation resulting in false data at the output. Silicon-germanium heterojunction bipolar transistor (SiGe HBT) technology has received extensive attention for its incorporation in extreme-environment electronic applications because of its excellent radiation tolerance, competitive high-speed operation (high f_T), ease of integration with traditional CMOS technology, and superb low-temperature performance. This work utilized SiGe HBT BiCMOS technology and employed radiation-hardening-by-design (RHBD) techniques to mitigate single event transients within microelectronics. The following is a summary of major contributions from this work:

1. An investigation on linearity of weakly-saturated and electrically matched SiGe NPN and PNP HBTs at room and elevated temperature. This work has been published in IEEE Silicon Monolithic Integrated Circuits in RF Systems (SiRF) 2014 [1].
2. Ultra low-frequency noise LDO voltage regulator utilizing C-SiGe HBT BiCMOS technology. This work has been published in IEEE International Symposium on Circuits and Systems (ISCAS) 2014 [2].

3. An investigation of single-event effects in C-SiGe HBT on SOI current mirrors. This work has been published in IEEE Transactions on Nuclear Science (TNS) 2014 [3].
4. A design technique to achieve a wide bandwidth without compromising the gain in a transimpedance amplifier (TIA) for optical communication. This work has been published in IEEE International Symposium on Circuits and Systems (ISCAS) 2013 [4].
5. Reducing single-event effects via internal and external negative feedback. This work has been presented at IEEE Nuclear and Space Radiation Effects Conference (NSREC) 2015, and its extension has been submitted to IEEE Transactions on Nuclear Science (TNS).
6. Systematic methodology for applying signal flow graph to analysis of feedback circuits. This work has been published in IEEE International Symposium on Circuits and Systems (ISCAS) 2014 [5].
7. Developing a high-speed analog to digital converter to reduce the structural complexity of a receive chain of radar systems.

CHAPTER 1

INTRODUCTION

1.1 SiGe HBT Technology

The silicon-germanium (SiGe) heterojunction bipolar transistor (HBT), fundamentally, is the same as a silicon (Si) bipolar-junction transistor (BJT) in structure except that band-gap engineering is utilized through the introduction of a graded germanium profile in the base layer. Fig. 1.1 shows the cross-section of a SiGe HBT. The corresponding doping and Ge profiles are shown in Fig. 1.2. The graded Ge profile results in a graded offset (slope) in the conduction energy band.

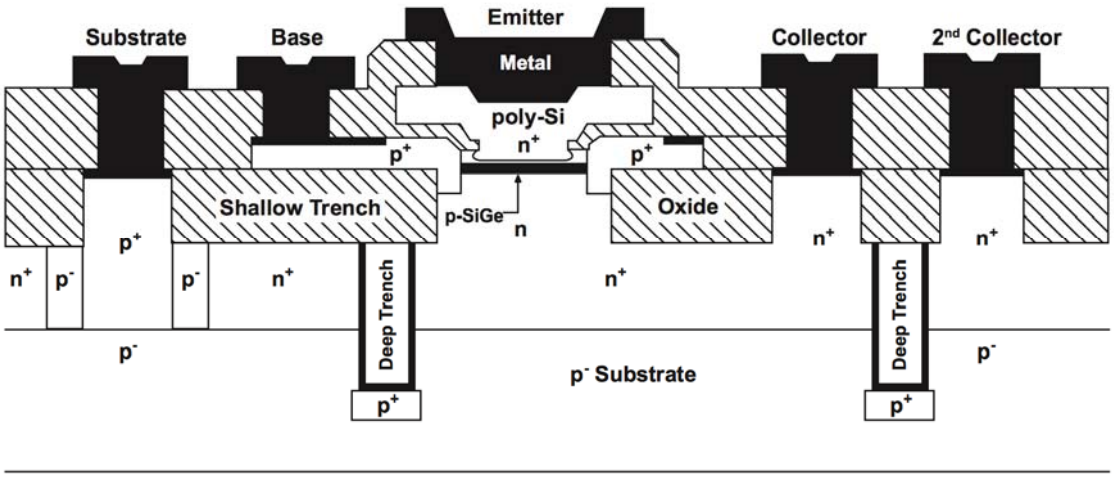


Fig. 1.1: Cross-sectional view of a SiGe HBT.

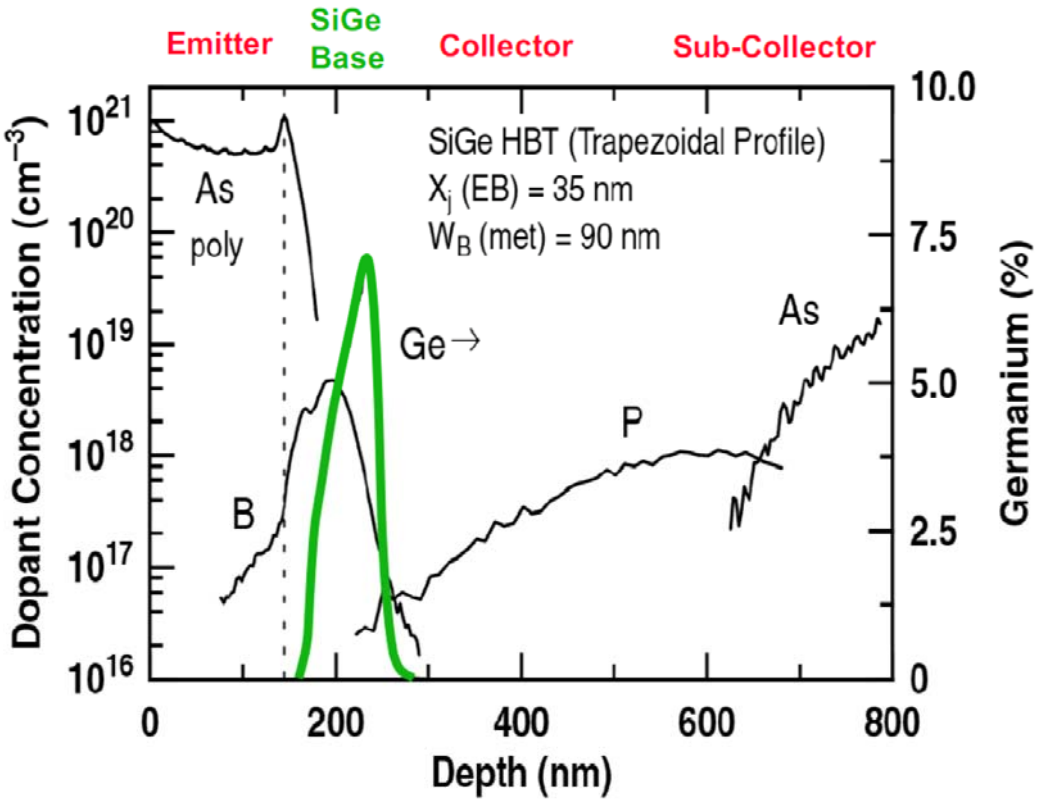


Fig. 1.2: Doping profile of first-generation SiGe HBT.

One of the major impacts of the graded conduction-band offset is to strengthen the minority-electron transport across the base region by creating a drift field. In addition, the potential barrier from the emitter to the base is reduced by the Ge content at the emitter-base junction, which leads to an exponential increase in electron injection for the same applied base-emitter voltage (V_{BE}), thereby increasing the current gain (β). The finite Ge content at the collector-base junction increases the Early voltage (V_A) because the smaller base bandgap near the collector-base junction weights the base profile; thus the back side depletion of the neutral base with increasing collector-base voltage is suppressed [6]. The drift field induced by the Ge grading causes a reduction in base transit time, which improves the AC response of the SiGe HBT. The enhanced injection

of electrons from the emitter into the base produces a back injection of holes from the base into the emitter; as a result, the emitter charge-storage delay time is reduced.

Due to this bandgap-engineering, SiGe HBTs enjoy improvements in current gain (β), Early voltage (V_A), and unity-gain frequency (f_T) over standard Si BJT counterparts. State-of-the-art NPN SiGe HBTs have been reported with peak f_T and f_{max} above 400 GHz at room temperature. This is a great motivation to utilize SiGe HBTs for high-speed analog and RF circuits. However, the relatively low breakdown voltage of SiGe HBTs can cause design challenges.

1.2 Electronics in Extreme Environments

Electronic systems often suffer from degraded performance or even fail after a length of time when operated in extreme environments. Radiation-induced damage is a major concern for modern semiconductor design platforms since technology scaling, i.e. the scaling down of the device structure and corresponding fabrication processes, can potentially lead to increased radiation sensitivity. The performance degradation can be caused by three primary mechanisms: 1) displacement damage, 2) ionization damage, 3) single-event effects (SEE). Displacement damage within silicon-based electronics is a function of the material system (rather than device layout, process parameters, feedback, etc.) and therefore will not be covered in the following discussion. Ionization damage within devices and circuits is usually addressed as total-ionizing-dose (TID) damage. SEE can be categorized as the various types of errors within a circuit; e.g., single-event transient (SET), single-event upset (SEU), multiple-bit upset (MBU), single-event latchup (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR).

1.3 Radiation Effects in SiGe HBTs

SiGe HBTs have become a strong contender for extreme-environment applications such as space-related electronics, which need to operate within radiation-intense and low-temperature environments, due to their inherent tolerance to multi-Mrad TID and excellent DC and AC performance at cryogenic temperatures. Increased base leakage does appear as a result of TID-induced damage, but this current is negligible because the magnitude of the change in current is very small. In addition, in order to mitigate SEE in SiGe-based circuits, a variety of device and circuit-level hardening techniques have been developed.

1.4 Research Objectives

The objective of this research is to investigate radiation-hardening-by-design (RHBD) techniques and apply them in circuit design to mitigate single-event effects utilizing SiGe HBT BiCMOS technologies. Chapter 2, 3, and 4 demonstrated the impressive improvements and performance of SiGe HBT due to bandgap-engineering in terms of low-frequency noise, linearity, and radiation tolerance, respectively. Chapter 5 discusses a methodology to increase the bandwidth of a transimpedance amplifier (TIA) without compromising the gain using complementary SiGe HBT technology. Chapter 6 investigates the negative feedback effects on SEE in circuits as a viable RHBD technique. Finally, in chapter 7, the findings made in chapter 6 are applied to a high-speed ADC to minimize SEE in its sub-analog components (high-speed comparator and high-speed D flip-flop).

CHAPTER 2

AN INVESTIGATION OF THE TEMPERATURE DEPENDENT LINEARITY OF WEAKLY-SATURATED, ELECTRICALLY MATCHED SIGE NPN AND PNP HBTS

2.1 Introduction

Low power consumption is often the driving constraint in applications such as biomedical devices, wireless transceivers, and battery operated systems. The typical approach to decreasing power in bipolar circuits in this context is to reduce the supply voltage to the bare minimum and then decrease the bias current, a tradeoff that inevitably results in performance loss. An alternative approach presented in [7], further reduces the supply voltage, forcing the device to operate in a weakly-saturated regime, while maintaining high current densities to achieve respectable RF performance. The present work investigates both NPNs and PNPs in the weakly-saturated regime, not only at room temperature, but also at an elevated temperature, for the first time, on an electrically-matched complementary SiGe BiCMOS on SOI platform. Electrically matched NPN and PNP SiGe HBTS are important in applications such as low voltage push-pull drivers and current feedback amplifiers.

This work utilizes a complementary silicon on insulator (SOI) technology [8], where the NPN and PNP devices are electrically matched such that both transistors have a similar peak cut-off frequency (f_T). The linearity performance of NPN and PNP SiGe HBTs is investigated in the weakly-saturated regime, at both room temperature (300 K) and an elevated temperature (373 K). In addition, the matched performance of these devices is compared in terms of power-gain and cut-off frequency, since such knowledge is crucial for circuits that must utilize both NPN and PNP HBTs in a symmetrical

manner. Finally, to better evaluate the linearity performance of these matched HBTs, a push-pull output stage of a current feedback amplifier (CFA) is designed and simulated in order to explore tradeoffs associated with operation in weak saturation. Simulation results indicate the output stage can be pushed into weak-saturation to reduce power, while maintaining low total harmonic distortion (THD).

2.2 Measurement Setup

Fig. 2.1 illustrates the fully-automated two-tone linearity measurement setup used in this study. The calibration and measurement procedure was as follows. First, the losses through multiple reference planes and the coupling factor of the directional coupler were measured, and a corresponding lookup table of losses was generated. Upon the construction of the lookup table, two-tone input signals were generated and applied to the device-under-test (DUT). The fundamental and third-order intermodulation (IMD3) products were measured on a spectrum analyzer. The clock signal of two function generators was synchronized to the clock signal of the spectrum analyzer to allow for 100 Hz span and 10 Hz resolution bandwidth measurements centered at each fundamental tone and IMD3 product.

A large source of tone power error was found to arise from the signal generators when sweeping large ranges of input power due to the power levels at which the internal step attenuator switches to different 10 dB attenuation bits. A power sensor on the coupled port of the directional coupler monitored the power level into the DUT, and any errors arising between the set tone power and the measured tone power was corrected for automatically utilizing a feedback loop in the MATLAB code. The additional isolator between the directional coupler and the input cable was used to prevent the reflection coefficient of the DUT from influencing the coupling factor of the directional coupler.

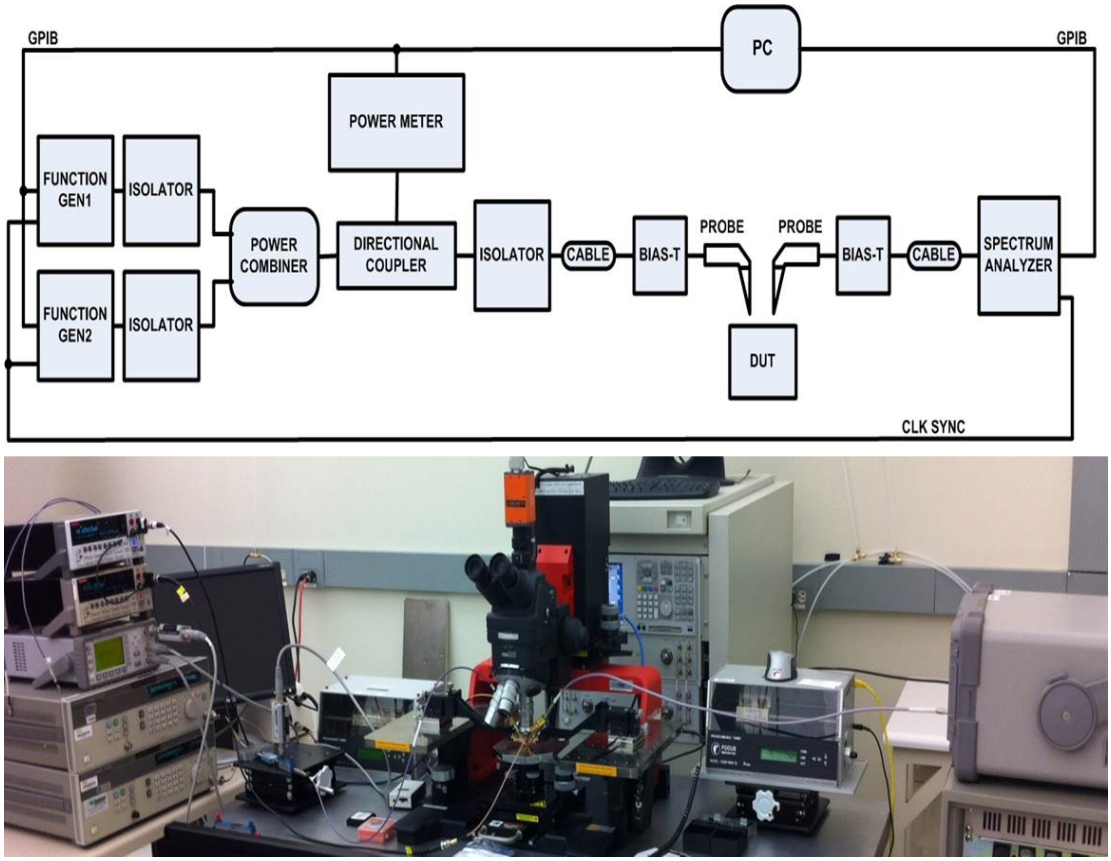


Fig. 2.1: Linearity measurement setup.

2.3 Experiments

2.3.1 Linearity at Room Temperature (300 K)

The measured cut-off frequencies (f_T) of the matched NPN and PNP HBTs at various V_{CE} are shown in Fig. 2.2. At high current density, the Kirk effect and heterojunction barrier effect occur and cause an increase in the total transit time, degrading f_T [9]. It is important to note that the peak f_T of the PNP occurs at a current density much higher than that of the NPN because for optimized performance, the collector of the PNP must be doped more heavily than the NPN in order to suppress the Kirk effect and heterojunction barrier effect. This inherently higher collector doping of

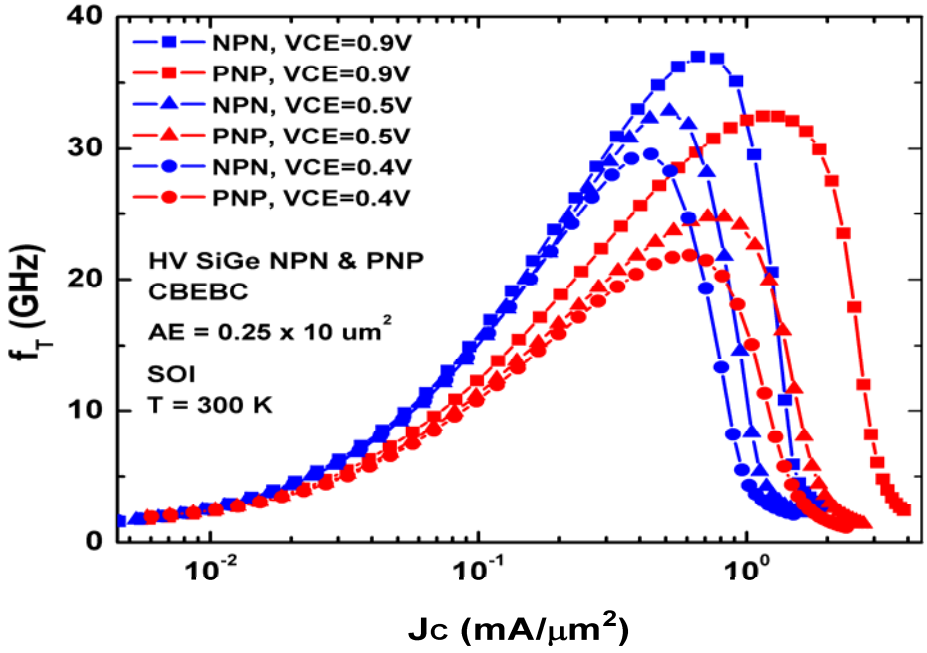


Fig. 2.2: Measured cut-off frequency (f_T) normalized to peak f_T vs. current density (J_C) at various V_{CE} of electrically matched SiGe NPN and PNP HBTs.

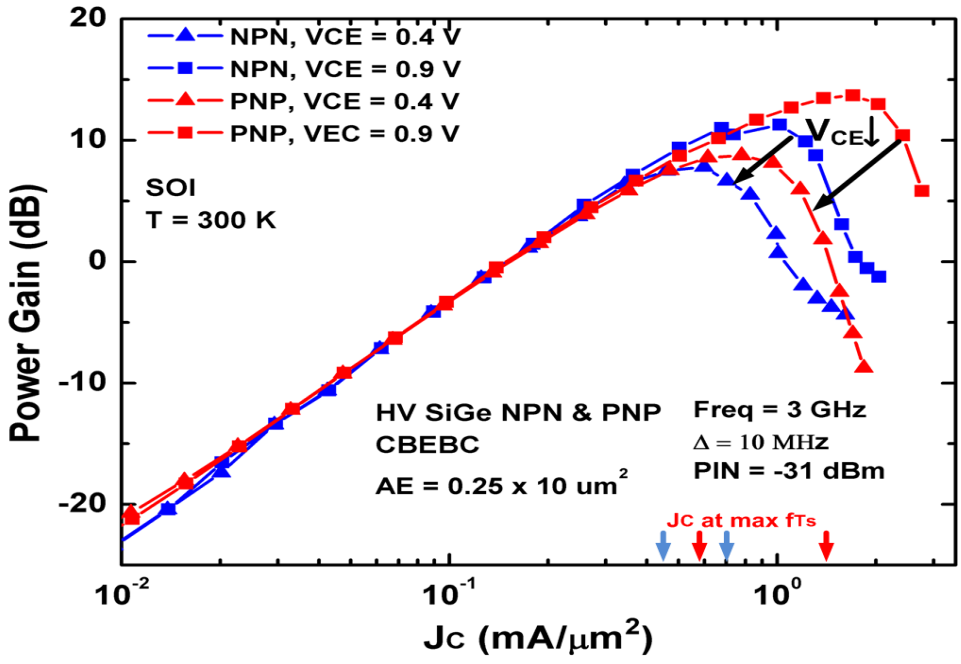


Fig. 2.3: Power-gain vs. current density (J_C) at various V_{CE} of electrically matched SiGe NPN and PNP HBTs at 300 K.

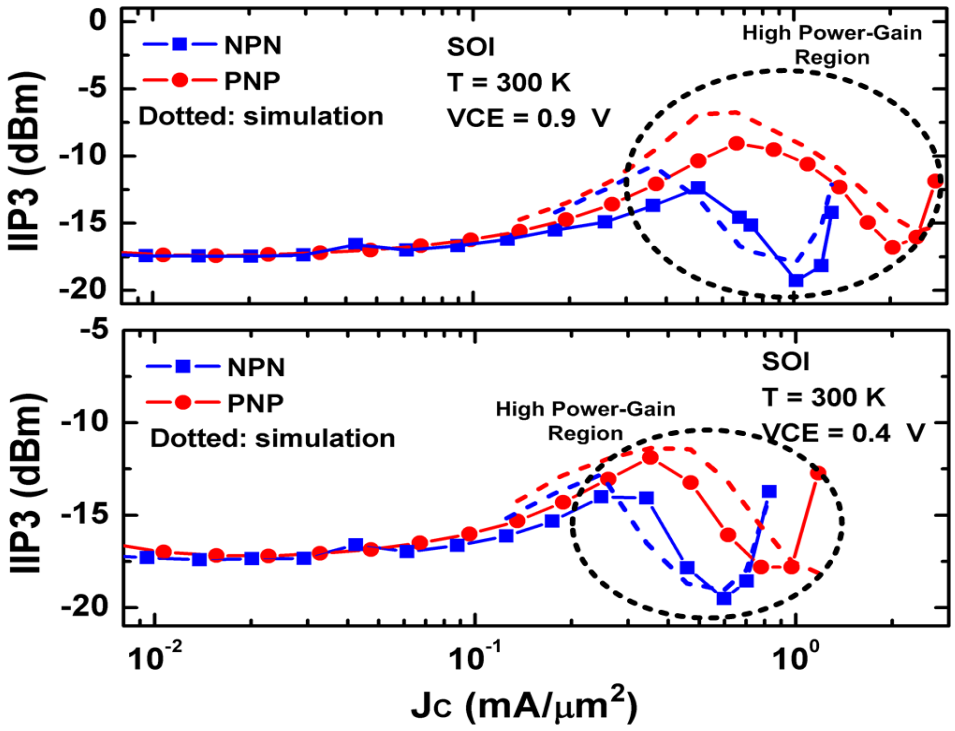


Fig. 2.4: IIP3 vs. current density (J_C) at various V_{CE} of electrically matched SiGe NPN and PNP HBTs at 300 K.

optimized PNP SiGe HBTs directly relates to the power-gain and IIP3 results, as will be shown.

Fig. 2.3 shows the power-gain of the NPN and PNP devices in both the forward-active (V_{CE} = 0.9 V) and weakly-saturated (V_{CE} = 0.4 V) regimes. The PNP exhibits slightly higher gain than the NPN, and it does not degrade until higher current densities. The current density for the maximum f_T of each device is indicated in Fig. 2.3.

The measured IIP3 results, obtained by injecting two tones with 10 MHz spacing at a center frequency of 3 GHz under 50 ohm matching conditions, are shown in Fig. 2.4. A higher V_{CE} improves linearity performance in the high gain region because the collector is more fully depleted [10]. The IIP3 also shows a similar phenomenon to the power gain, in which the PNP exhibits higher linearity than the NPN at high current

densities. Fig. 2.4 also shows good correlation between simulated and measured IIP3 and validates the models within the process design kit for the weak-saturation region.

The observed differences between the NPN and the PNP devices can be explained by the physical difference in the doping profiles required to produce an electrically matched performance. The linearity performance differs mainly because the higher doping concentration in the collector (N_C) of the PNP causes C_{CB} to be more resistant to changes in the voltage between the collector and the base (V_{CB}) [11]. As a result, PNPs have improved linearity under similar bias conditions, a fact that can be exploited at the circuit level.

2.3.2 Elevated Temperature Effects on Linearity

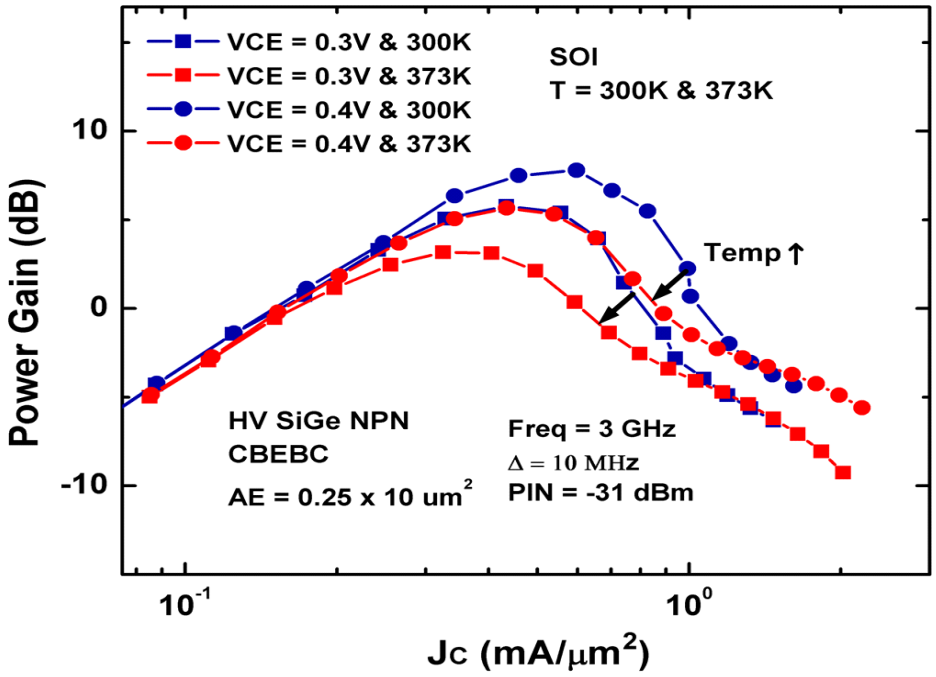


Fig. 2.5: Power-gain vs. current density (J_C) at various V_{CE} of electrically matched SiGe NPN HBT at 300 and 373 K.

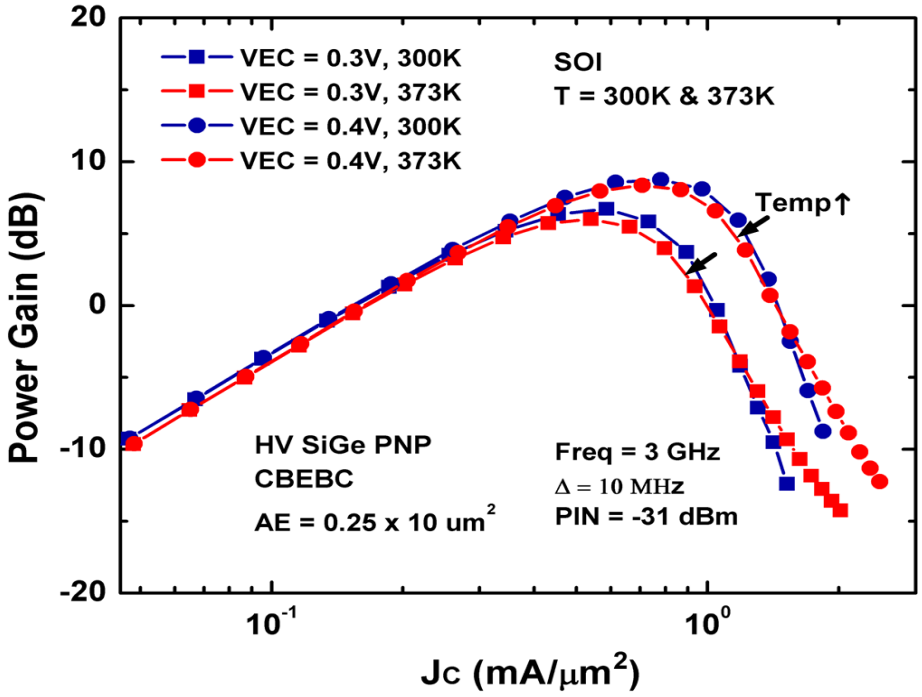


Fig. 2.6: Power-gain vs. current density (J_C) at various V_{CE} of electrically matched SiGe PNP HBT at 300 and 373 K.

Figures 2.5 and 2.6 show shifts in the power-gain of the NPN and the PNP SiGe HBTs in the weakly-saturated (V_{CE} = 0.3 V and V_{CE} = 0.4 V) region when the temperature is raised to 373 K from room temperature (300 K). For a fixed bias current, the junction turn-on voltage and the transconductance (g_m) decrease when the temperature rises [12]. The reduction in g_m results in a corresponding decrease in the power-gain.

The PNP exhibits less degradation in the power-gain than the NPN as the temperature increases. This is reflected in the IIP3 performance at the elevated temperature, as shown in Fig. 2.7. The shift of the PNP IIP3 versus the collector current density at the elevated temperature is smaller than that of the NPN (ΔJ_{C_PNP} and ΔJ_{C_NPN},

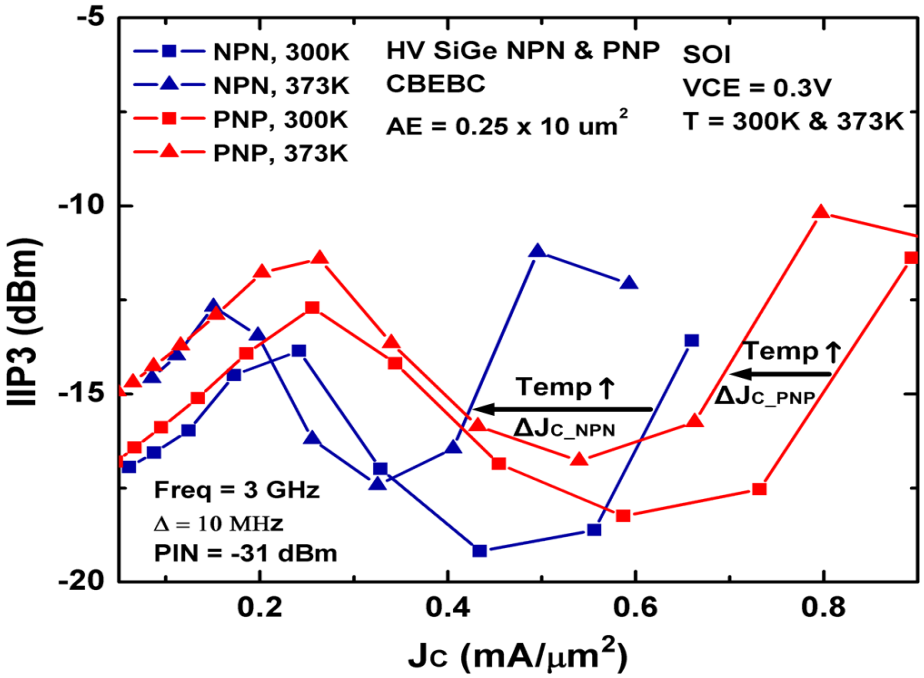


Fig. 2.7: IIP3 vs. current density (J_C) at various V_{CE} of electrically matched SiGe NPN and PNP at 300 and 373 K. J_C is on a linear-scale.

respectively). The data are plotted on a linear scale and zoomed-in on the high power-gain region for comparison purposes.

2.4 Circuit Applications

In order to better investigate the feasibility of using the electrically matched NPN and PNP devices in weak-saturation, the push-pull output stage of a current feedback amplifier (CFA) was designed and simulated using the design kit models (which are well-calibrated in weak saturation).

Fig. 2.8 shows the input stage and the push-pull output stage of a typical current feedback amplifier [13]. As illustrated in the complementary symmetrical architecture of

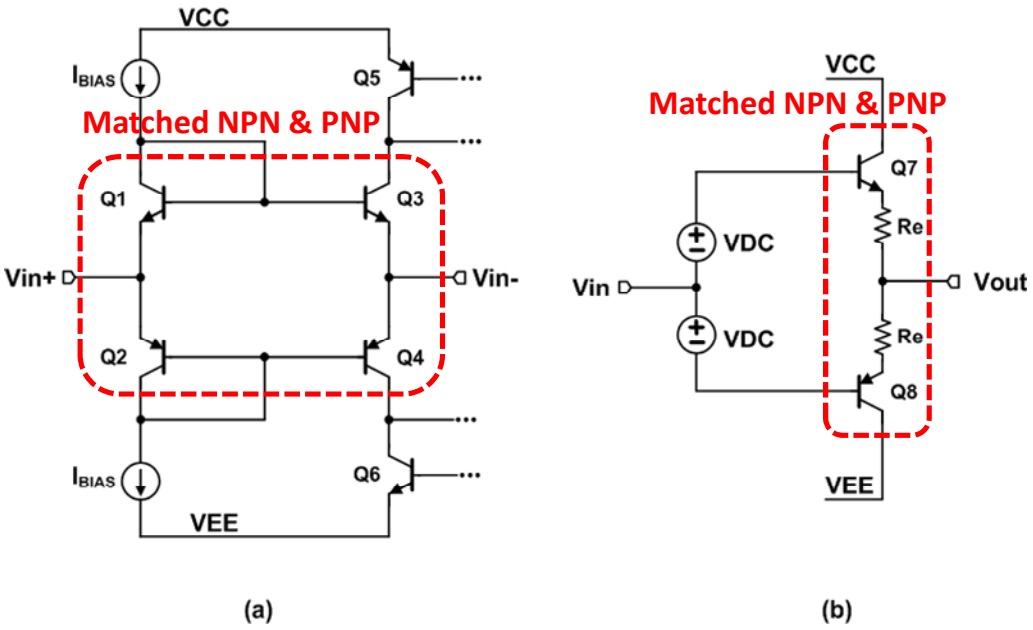


Fig. 2.8: Input stage (a) and push-pull output stage (b) of a current feedback amplifier utilizing electrically matched SiGe NPN and PNP HBTs.

Table 2.1: Summary of Push-pull Performance

Supply	THD/300K	THD/373K	P_{DC}
2 V	< 1 %	< 1 %	28.0 µW
1.2 V	< 1 %	1.57 %	16.8 µW
1 V	1.12 %	3.83 %	14.0 µW
0.8 V	4.34 %	6.26 %	11.2 µW

the CFA, it is crucial that the NPN and PNP have an electrically matched performance to achieve optimum performance. The push-pull output stage in Fig. 2.8 (b) was designed

with class AB biasing. Total Harmonic Distortion (THD), a key design metric dependent upon intrinsic linearity of the underlying devices, was simulated as V_{CE} decreased into weak saturation, at both 300 and 373 K. The fundamental frequency was set at 100 MHz. Table I summarizes the results.

THD remains less than 1 % at 300 K when the supply voltage drops to 1.2 V from 2.0 V, which is equivalent to V_{CE} of 0.6 V (weak-saturation). THD increases, however, to 1.6 % at 373 K for the same supply voltage (1.2 V). As the supply voltage is further reduced, THD rises. Note, however, that the DC power consumption dramatically reduces as the devices enter into deeper saturation region. When the supply voltage drops to 0.8 V at 373 K, THD becomes larger than 5 %, which is considered to be the maximum acceptable distortion [14].

2.5 Summary

The linearity of an electrically matched NPN and PNP SiGe HBTs in the weakly-saturated region was investigated for low power applications at 300 K and 373 K, for the first time. Electrically matched performance is crucial for applications in which both the NPN and the PNP are necessary components due to their symmetrical structure, such as in low-voltage drivers and current feedback amplifiers. The measurement results verified the feasibility of utilizing them in the weakly-saturated region to reduce power consumption. In addition, the simulation results of a class AB push-pull output stage demonstrate the complementary NPN and PNP devices can be pushed into the weakly-saturated region, while maintaining low THD.

2.6 Acknowledgement

Seungwoo Jung would like to thank Texas Instruments SiGe team for their support.

CHAPTER 3

A COMPLEMENTARY SIGE HBT ON SOI LOW DROPOUT VOLTAGE REGULATOR UTILIZING A NULLING RESISTOR

3.1 Introduction

Low-dropout (LDO) regulators are essential building blocks in numerous electronic applications, since they function as power management ICs. It is crucial that such regulators provide a low dropout voltage for low supply voltage applications, where demand is rapidly increasing.

Complementary SiGe HBTs (C-SiGe HBTs) have some unique advantages over CMOS for reducing dropout voltages and low-frequency noise. The high current gain (β) enables the output PNP device to deliver a large current to a load without causing a significant dropout voltage, when compared with PMOS output devices of a similar size. In addition, the low-frequency noise performance of SiGe HBTs is superior to that of CMOS transistors (by orders of magnitude). The two most commonly used PNP SiGe HBTs in the present technology platform, a CBEBC (Collector-Base-Emitter-Base-Collector) and BEC (Base-Emitter-Collector) configuration, have been reported to possess different Early voltages (V_A), with the V_A of the CBEBC device larger than V_A of the BEC device [15]. Inspired by this result, the present work also investigates the feasibility of reducing dropout voltages and possibly low-frequency noise further by comparing both PNP SiGe HBT options (CBEBC vs. BEC) as an output device in the design process of LDO regulators.

Based on the required specification of an instantaneous peak dropout voltage of 15 mV at the output current of 150 mA, the off-chip load capacitor value was determined to be 100 μF. However, this large capacitor causes the LDO regulator to be unstable by

producing a LHP zero at a very low frequency. To overcome the instability, a nulling resistor in series with a Miller capacitor is employed in order to ensure a sufficient phase margin by converting a RHP zero (caused by the Miller capacitor) to a LHP zero.

Signal flow graphs are utilized here to obtain accurate equations for the converted zero and the Miller pole that reflects the effects of the nulling resistor R_Z through a HBT inverting gain stage in order to insert them in the desired places. The derivation of these equations is conducted without any of the assumptions commonly made in literature. For instance, in [16-17] the converted zero and Miller pole equations with R_Z for a CMOS inverting gain stage is shown, but with important assumptions.

3.2 LDO Design Employing Nulling Resistor

Fig. 3.1 shows the LDO regulator architecture. Two LDO regulators were designed, deviating only in the output devices used (Qout): CBEBC and BEC PNP SiGe HBTs on SOI [18]. Design challenges arise from the fact that the 100 μF off-chip load capacitor C_L produces a LHP zero at a very low frequency and reduces the phase margin significantly by keeping the loop-gain from falling into the low-frequency band.

Fig. 3.2 illustrates the loop-gain and phase response of the LDO regulator without the internal compensation capacitor C_C, for the series parasitic resistance $R_P = 0$ and $R_P \neq 0\ \Omega$. When $R_P = 0$, the phase margin is greater than 90 degrees because the large off-chip load capacitor sets the dominant pole at a very low frequency, and the loop-gain falls continuously from the cut-off frequency (black solid line in Fig. 3.2). As a result, the loop-gain crosses the unity gain frequency (0 dB) before the other poles are encountered, ensuring sufficient phase-margin. With $R_P \neq 0\ \Omega$, however, a LHP zero is introduced into the system as the load capacitor is getting shorted. This zero keeps the loop-gain from decreasing in the low-frequency band and lets it fall in the higher frequency band where multiple poles are located (red solid line in Fig. 3.2). When multiple poles are encountered, the phase drops quickly, to the point that the phase margin is insufficient to

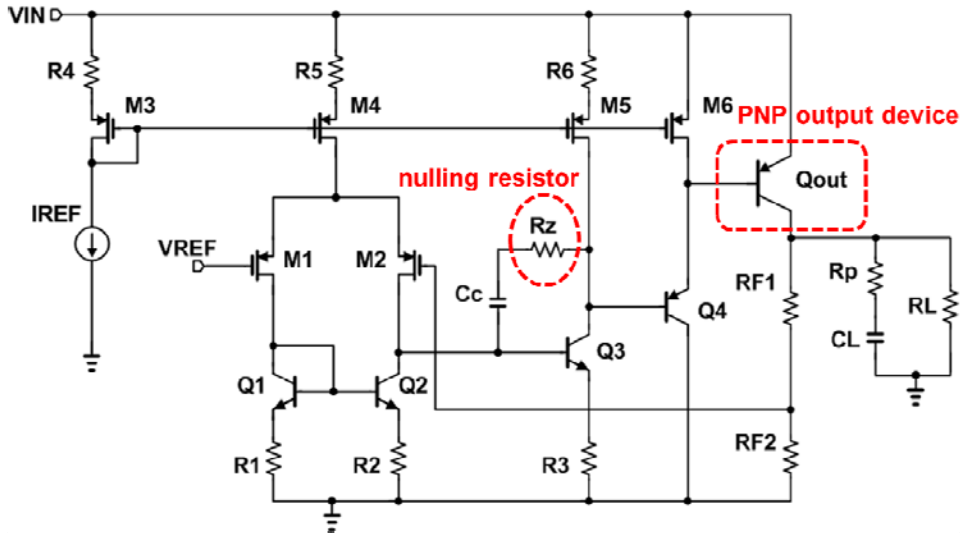


Fig. 3.1: Low Drop Out (LDO) voltage regulator with CBEBC and BEC PNP HBT output devices (Qout). The nulling resistor Rz converts a right-hand plane (RHP) zero caused by the inverting gain stage (Q3) and Miller capacitor Cc to a left-hand plane (LHP) zero.

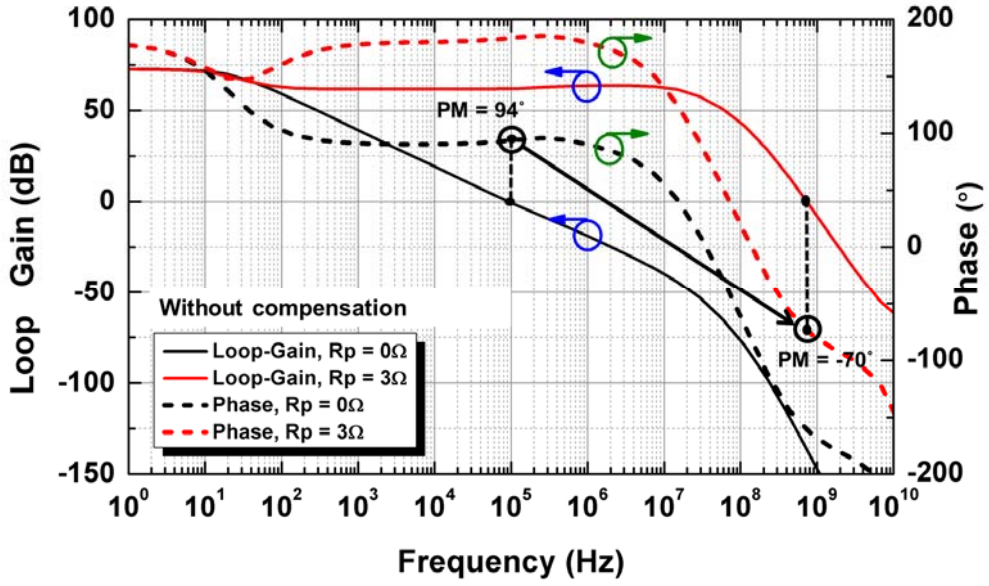


Fig. 3.2: Simulated loop-gain and phase responses of the LDO regulator without the compensation capacitor Cc. The black lines are for $R_P = 0$, and the red lines are for Rp = 3 Ω. R_P is the parasitic resistance in series with the load capacitor C_L.

guarantee the stability before the loop-gain crosses unity gain frequency. The phase margin changes from 94˚ to -70˚ when R_P changes from zero to 3 Ω, as shown in Fig. 3.2.

To provide a sufficient phase margin for the stability, the LDO regulator is compensated with a Miller capacitor C_C to bring the second pole (Miller pole) close to the LHP zero caused by the off-chip capacitor, such that the loop-gain can start to fall earlier in the low-frequency band, cancelling the effects caused by the LHP zero, as shown in Fig. 3.3. The phase margin is increased to 44˚ from -70˚ degrees with C_C at the unity gain frequency, but this value is still not sufficient to ensure the stability (the black lines in Fig. 3.3). The phase margin is further improved by inserting a nulling resistor (R_Z) in series with C_C. With R_Z, a RHP zero caused by Cc and the inverting gain stage is converted to a LHP zero as C_C is being shorted.

In order to insert the converted LHP zero as well as the Miller pole with R_Z at the desired frequencies, the complete transfer function is derived by utilizing signal flow graphs, without any assumptions or simplifications. The common emitter inverting gain stage (with C_C and R_Z) and the equivalent circuit with the feedback network replaced with the *Thevenin* circuit for ac analysis are shown in Fig. 3.4 (a) and (b), respectively. Based on Fig. 3.4 (b), the signal flow graph is constructed as shown in Fig. 3.5 [4], [18]-[19].

By inspection of the flow graph, the transmission gain (transfer function) can be expressed as

$$\frac{v_{out}}{v_{in}} = \frac{-g_m r_\pi R_L \left[\left(R_z - \frac{1}{g_m} \right) c_c s + 1 \right]}{(r_\pi + R_{in}) \left[(R_L + R_z + R_{in} \| r_\pi + g_m R_L R_{in} \| r_\pi) C_c s + 1 \right]} \quad (1)$$

The LHP zero and the Miller pole frequencies can be attained as

$$\omega_{LPZ} = \frac{-1}{\left(R_z - \frac{1}{g_m}\right)C_c} \tag{2}$$

$$\omega_P = \frac{-1}{\left(R_L + R_z + R_{in} \| r_\pi + g_m R_L R_{in} \| r_\pi\right)C_c} \tag{3}$$

Interestingly, the solution for the converted LHP zero of the HBT inverting gain stage in (2) is identical as that from the CMOS inverting gain stage [16-17].

Using equation (2), the values for R_Z, g_m, and C_C are chosen to insert the LHP zero between 30 and 40 MHz. As shown in Fig. 3.4, the converted LHP zero increases the phase (dotted red line), resulting in a phase margin of 99°.

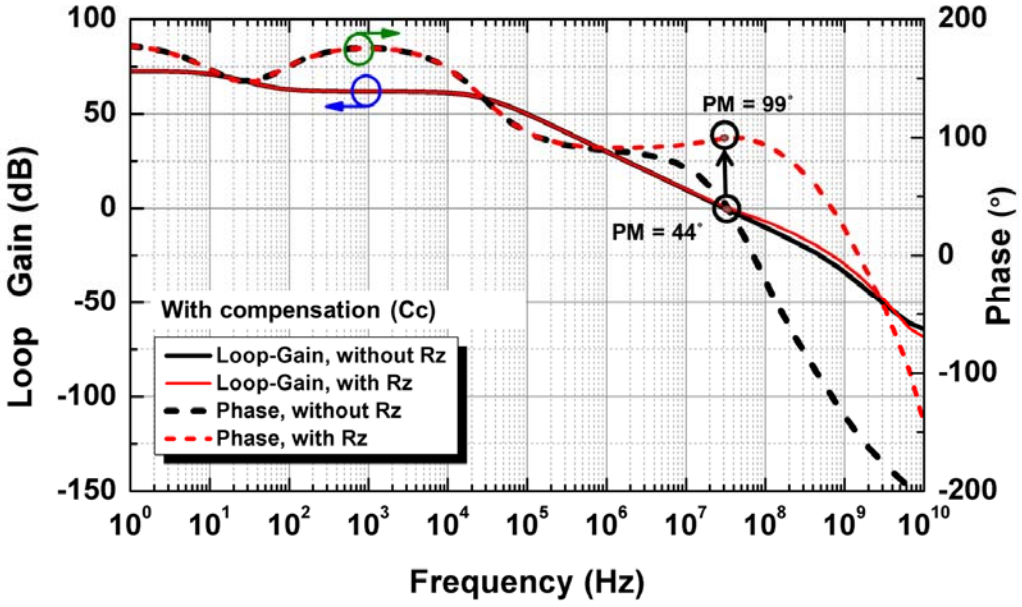


Fig. 3.3: Simulated loop-gain and phase responses of the LDO regulator with the compensation capacitor Cc. The black lines are for Rz = 0, and the red lines are for Rz ≠ 0.

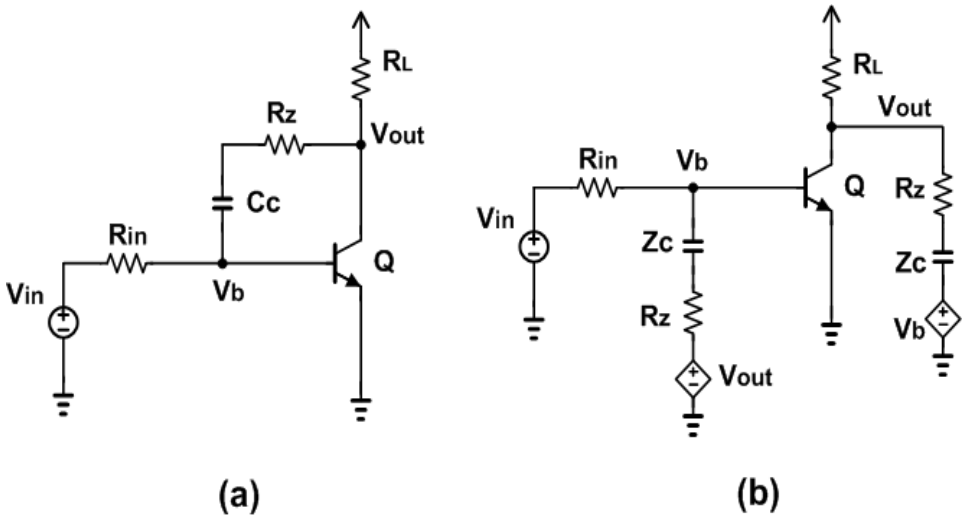


Fig. 3.4: (a) The inverting gain stage of the LDO regulators with the compensation capacitor Cc and the nulling resistor Rz. (b) The equivalent circuit with the feedback network replaced with the *Thevenin* circuits for ac analysis.

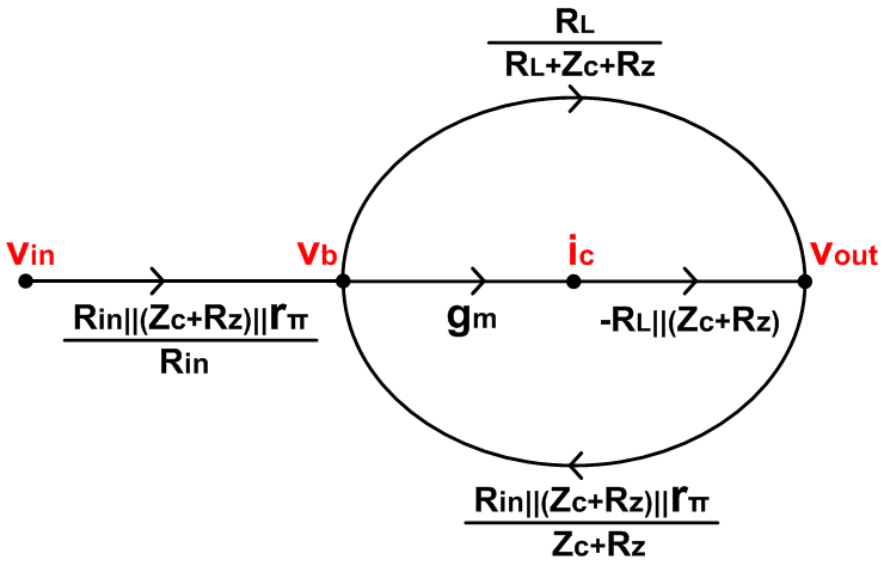


Fig. 3.5: Signal flow graph is constructed based on Fig. 3.4 (b) for an ac analysis.

3.3 Measurements

Two C-SiGe LDO regulators were fabricated with the output devices configured as either arrays of (Qout in Fig. 3.1) CBEBC or BEC PNP HBTs in order to investigate their unregulated dropout voltage and low-frequency noise performance. The die photo of the LDO regulator is shown in Fig. 3.6. Thirty-two devices of each kind (each with an emitter area = 1.25 x 10 μm^2) were integrated in parallel to deliver over 100 mA from the LDO. Fig. 3.7 shows the top view of the CBEBC (a) and BEC (b) PNP HBTs [18]. The measurement setup is shown in Fig. 3.8.

The dropout voltages with V_{IN} = 2.0 and 2.5 V were measured as the output current was increased, and the results are shown in Fig. 3.9. We note that the dropout voltage performance was optimized at V_{IN} = 2 V for the design process. The rate of the output voltage drop increases as the output current rises, because the open-loop gain of the LDO decreases when the load resistance decreases. The dropout voltage of the LDO regulator with CBEBC is less than the dropout voltage of the LDO with BEC PNP HBTs as the output current value increases for both V_{IN} = 2.0 and 2.5 V, as shown in Fig. 3.9, because the Early voltage (V_A) of CBEBC is higher than that of the BEC HBT [15]. Table 3.1 summarizes the dropout voltage values at high output currents and shows a significant improvement in the dropout voltages of the regulator with CBEBC PNP output devices compared to the one with BEC PNP output devices.

The low-frequency noise voltage spectral densities (in V^2/Hz) for both C-SiGe LDO regulators were measured utilizing an Agilent 35670A dynamic signal analyzer and are plotted in the frequency range between 1 Hz and 100 kHz in Fig. 3.10. From the data, it is observed that the differences in the low frequency noise performance between the two regulators with CBEBC and BEC PNP HBT output devices are minimal. In a frequency band less than 10 kHz, flicker noise is the dominant noise source; however, shot noise becomes the principal noise beyond 10 kHz in both circuits.

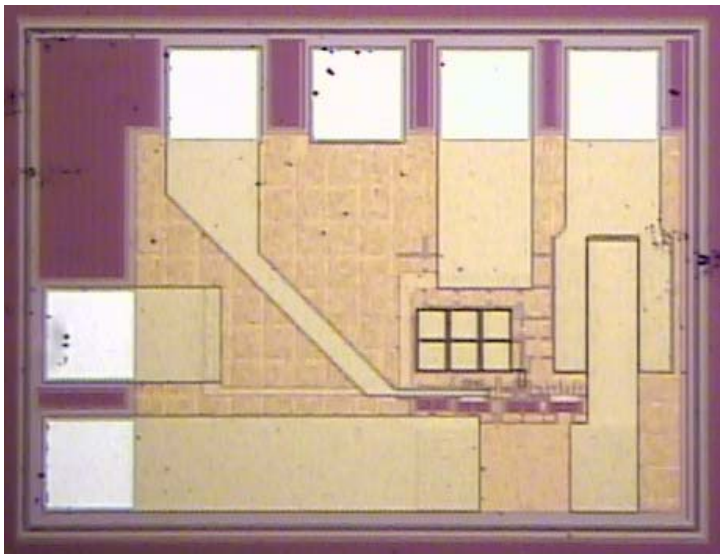


Fig. 3.6: The LDO regulator die photo.

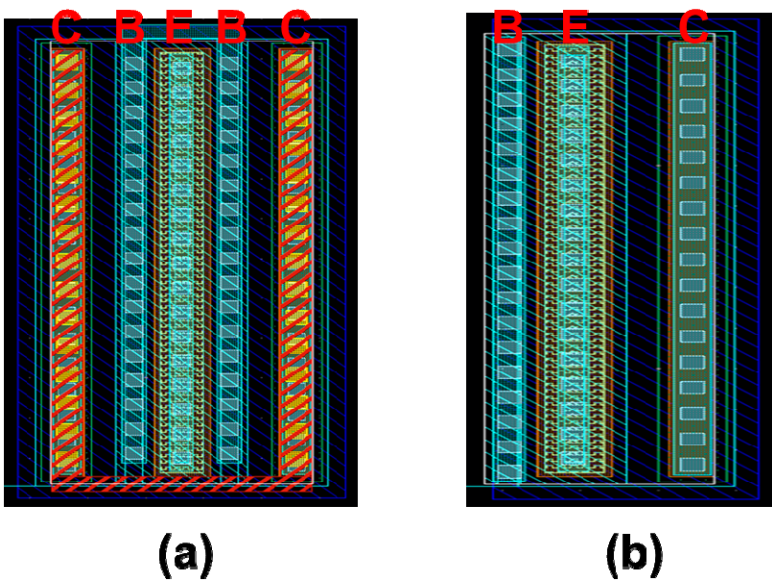


Fig. 3.7: (a) Top view of CBEBC SiGe PNP HBT on SOI. (b) Top veiw of BEC SiGe PNP HBT on SOI.

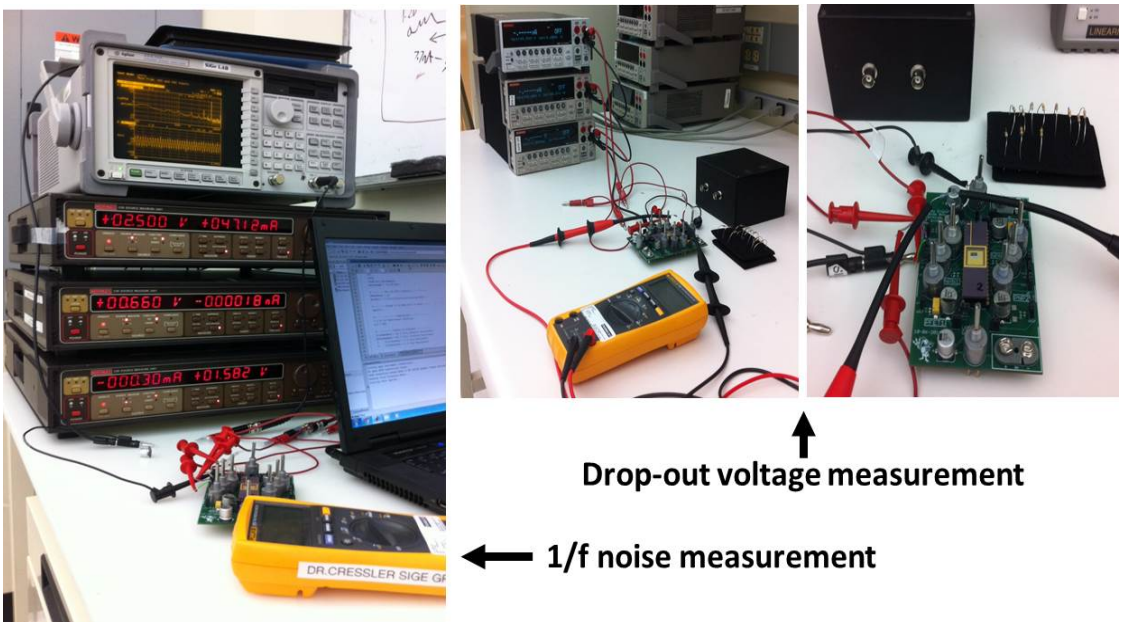


Fig. 3.8: 1/f noise and drop-out voltage measurment setup.

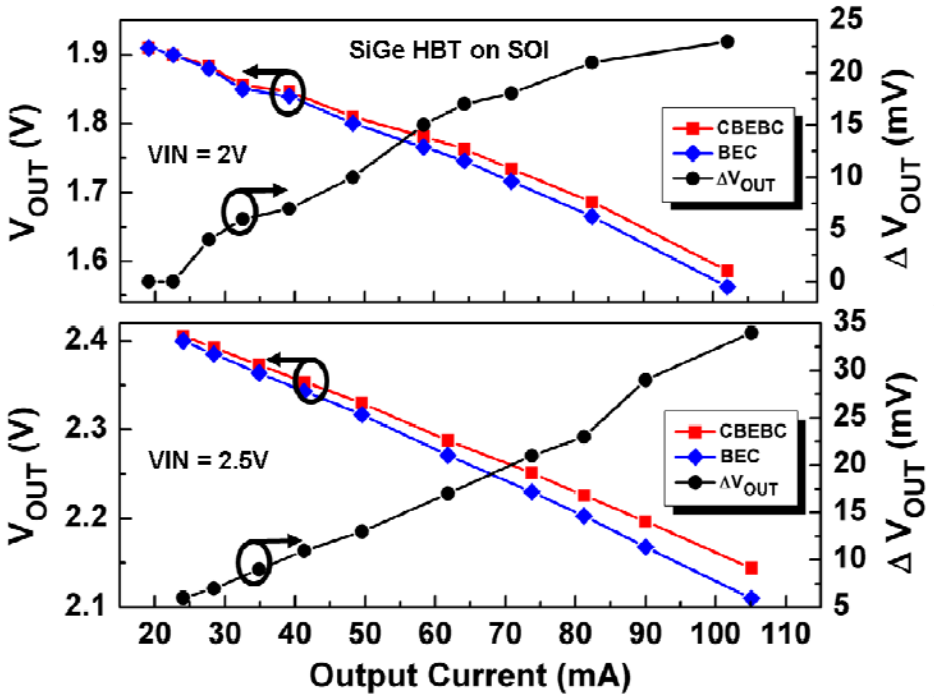


Fig. 3.9: The ouput current versus dropout voltage with VIN = 2 and 2.5 V. The LDO regulator with CBEBC PNP output devices exhibits less dropout voltage values than the one with BEC PNP ouput devices. ΔV_{OUT} = (V_{OUT} of CBEBC) – (V_{OUT} of BEC).

Table 3.1: Dropout Voltages of CBEBC and BEC Output PNP SiGe HBTs

	IOUT					
	80 mA		90 mA		103 mA	
	CBEBC	BEC	CBEBC	BEC	CBEBC	BEC
Dropout(mV), Vin = 2.0 V	215	236	237	254	266	284
Dropout(mV), Vin = 2.5 V	274	297	303	332	356	390

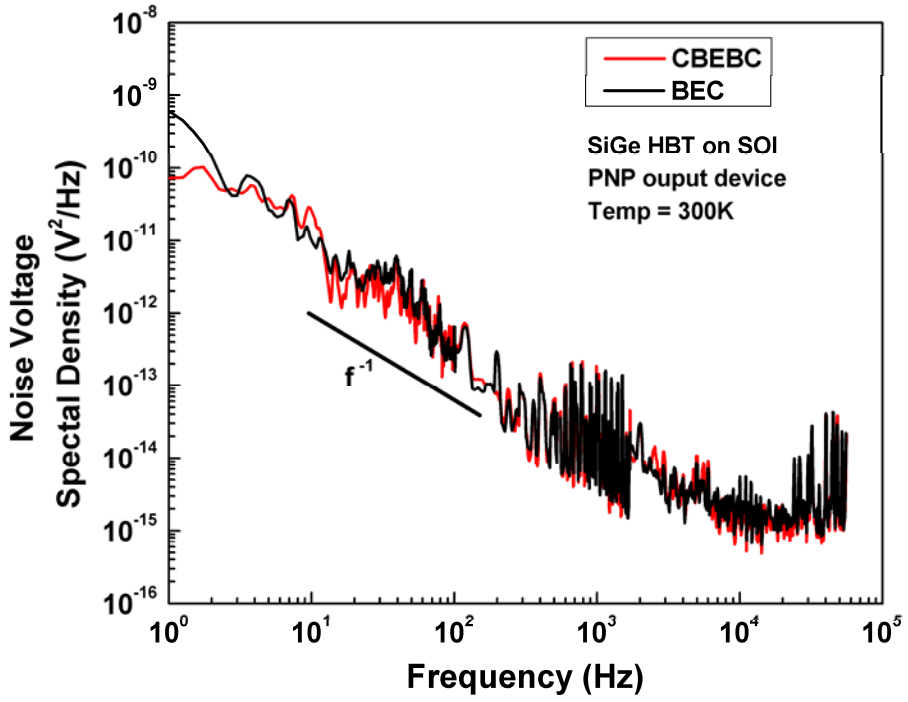


Fig. 3.10: The noise voltage spectral density in the frequency band between 1 Hz and 100 kHz is measured utilizing Agilent 35670A Dynamic Signal analyzer.

Table 3.2 compares the performance of the presented C-SiGe LDO regulator with the CBEBC PNP output device, with the performance of other state-of-the-art LDO

regulators [20]-[22]. The dropout voltage of the C-SiGe LDO regulator presented here is comparable, and the low frequency noise performance is superior, to that of other state-of-the-art LDO regulators.

Table 3.2: LDO Voltage Regulator Performance Comparisons

	[8]	[9]	[10]	THIS WORK
V_{IN}	3.00 V	1.15 V	2.70 V	2.00 V
I_{O_MAX}	50 mA	25 mA	200 mA	103 mA
Dropout	200 mV	150 mV	230 mV	266 mV
PSRR	57 dB	56 dB	58 dB	45 dB
Noise at 100 Hz	4.6 μV/√Hz	NA	2.4 μV/√Hz	0.55 μV/√Hz
Technology	CMOS	CMOS	BiCMOS	C-SiGe HBT

3.4 Summary

In this work, a commercially-available complementary SiGe HBT on insulator (SOI) technology was utilized to reduce the dropout voltages and low-frequency noise of LDO regulators. The feasibility of reducing the dropout voltage and noise even further by employing different types of PNP output devices was also explored. Measured results indicate that the dropout voltages can be improved by employing the CBEBC PNP output device over a BEC PNP output device. However, the differences in the low-frequency noise between the LDO regulators with the two different PNP output devices were minimal. The dropout voltage was comparable, and the low frequency noise performance was superior, to state-of-the-art LDO regulators presented in [8-10].

The complete transfer function to predict the positions of the converted LHP zero and the Miller pole affected by the nulling resistor was derived using signal flow graphs, importantly, without any assumptions commonly made in literature.

3.5 Acknowledgement

Seungwoo Jung is thankful to Texas Instruments SiGe team for their support.

CHAPTER 4

AN INVESTIGATION OF SINGLE-EVENT TRANSIENTS IN C-SIGE HBT ON SOI CURRENT MIRROR CIRCUITS

4.1 Introduction

Silicon-germanium heterojunction bipolar transistor (SiGe HBT) technology has received extensive attention for incorporation in extreme-environment electronic applications because of its excellent total-ionizing-dose radiation tolerance, competitive high-speed operation (high f_T), ease of integration with traditional CMOS technology (only a small number of extra mask layers required), and superb low-temperature performance [23]-[30]. However, investigations have also shown that the SiGe HBT technology is susceptible to single-event effects (SEE), the worst case being in high-speed digital circuits; low linear energy transfer thresholds and high saturated error cross-sections have been reported for digital shift registers fabricated utilizing first-generation SiGe HBTs [31]-[32].

In order to lessen the sensitivity of SiGe HBTs to SEEs, the characterization of transient currents and identification and development of various hardening methodologies, both at the device and circuit levels, have been investigated [33]-[41]. It has been demonstrated that the SiGe HBTs under inverse-mode operation (emitter and collector terminals swapped) as a device-level radiation-hardening-by-design (RHBD) technique have improved SEU sensitivity in high-speed digital circuits and cascode SiGe HBTs [42]-[43].

Unlike bulk technology, the transistors in SiGe HBT on SOI technology are insulated by a buried oxide composed of deep trench (DT) isolation and SOI [8], [15]. This device level isolation technique in SOI technology has potential for improving SEU

sensitivity significantly in the circuit (or system) level because the isolation can prevent ion-strike induced transient currents from entering into adjacent SiGe HBTs; whereas, transistors in bulk technology are directly affected by transient currents through the common substrate.

In the present work, the single-event response of various current mirror circuits designed and fabricated utilizing the Texas Instruments CBC-8 C-SiGe HBT on SOI technology is investigated. Current mirror circuits are chosen as the subject of the investigation because they are one of the most essential and fundamental DC biasing blocks in integrated circuits. Virtually all analog and RF circuits utilize current mirrors for their DC biasing. Thus, understanding the behavior of commonly employed current mirrors w.r.t. single events transients is crucial for designing extreme-environment electronic systems. We utilized Texas Instruments CBC-8 C-SiGe HBT on SOI technology platform for this study since it offers both high performance SiGe NPN and PNP HBTs and DT/SOI isolation [8], [15], [44].

4.2 Current Mirrors

A current mirror is a circuit block designed to produce a copy of a current (reference current I_{REF}) in the output terminal of one active device (Q2 and M2 in Fig. 4.1) by controlling the current in another active device (Q1 and M1 in Fig. 4.1). SiGe HBT and MOS basic current mirrors are shown in Fig. 4.1 (a) and (b), respectively. The collector current in the SiGe HBT current mirror is given as

$$i_C = I_S\left(e^{\frac{v_{BE}}{V_T}} - 1\right)\left(1 + \frac{v_{CE}}{V_A}\right) \tag{1}$$

where I_S is the reverse saturation current on the order of 10^{-15} to 10^{-12} A, V_T is the thermal voltage (approximately 26 mV at 300 K), and V_A is the Early voltage.

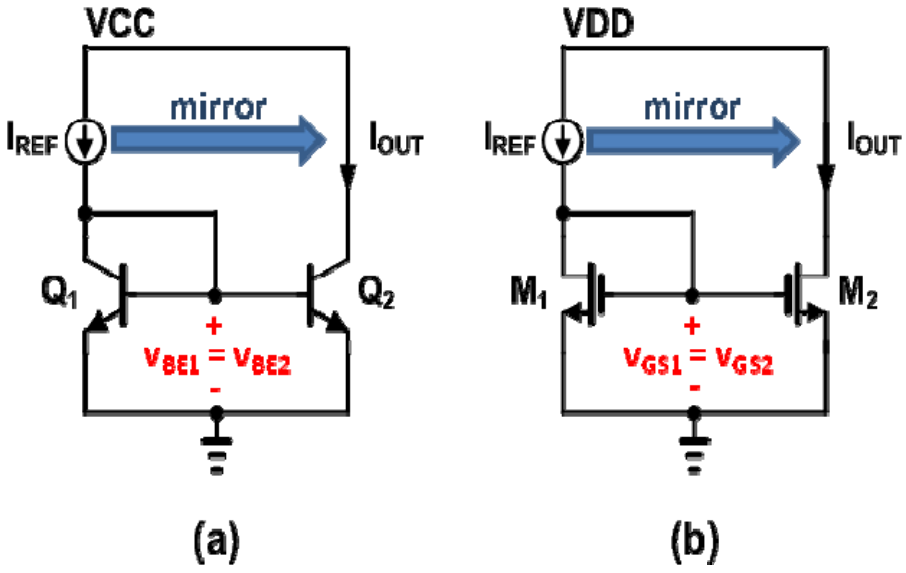


Fig. 4.1: Basic SiGe HBT NPN current mirror (a) and basic NMOS current mirror (b).

As shown in equation (1), the collector current is an exponential function of the base-emitter (v_{BE}) junction voltage and a linear function of the collector-emitter voltage (v_{CE}); in addition, the Early voltage V_A is much larger than the collector-emitter voltage. Thus, the collector current of a SiGe HBT is predominantly determined by the base-emitter junction voltage. Current mirrors utilize this fact to mirror the reference current to the output terminal; i.e. as long as the base-emitter voltages of two SiGe HBTs are equal ($v_{BE1} = v_{BE2}$), the collector current of those devices must be identical ($i_{C1} = i_{C2}$), assuming the effects of v_{CE} to the collector current is negligible.

Fig. 4.2 illustrates how the mirrored reference current (I_{REF}) is utilized to DC bias various circuits within an integrated circuit. The dotted red rectangular region represents

the various parts of an integrated circuit that need to be DC biased. The magnitude of individual DC bias current I_{OUTn} (n is an integer) can be set independently by selecting the corresponding device size (i.e., emitter area). The total output current I_{OUT} in the figure is regulated by a voltage regulator.

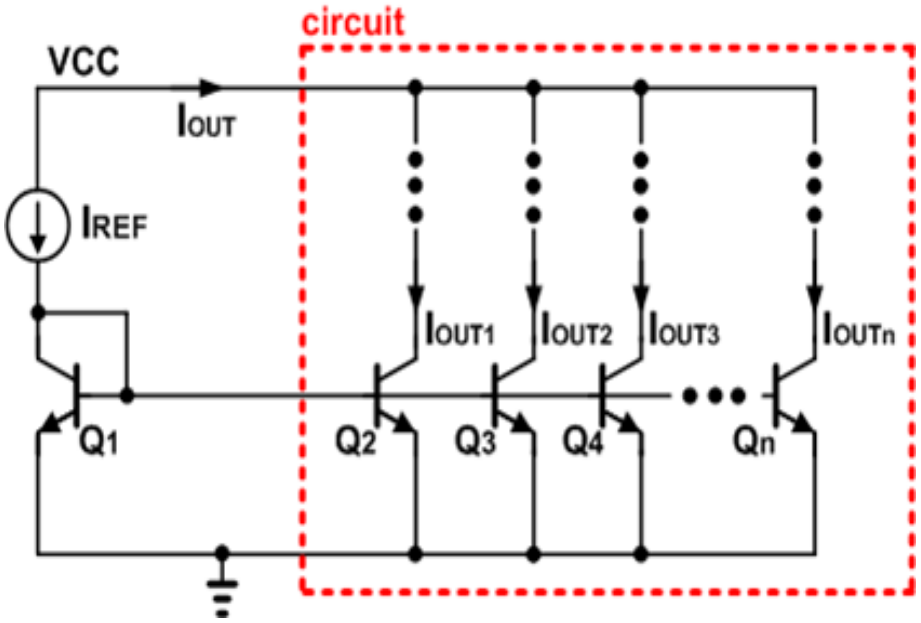


Fig. 4.2: Illustration that shows how the mirrored reference current I_{REF} can DC bias various regions of an integrated circuit.

Four different types of current mirrors were investigated: basic NPN, cascode NPN, basic PNP, and inverse-mode PNP current mirror (Fig. 4.3). Except for the inverse-mode PNP current mirror, the other three current mirrors are commonly utilized in integrated circuit design for DC biasing; however, note that PNP current mirrors are only available in the platforms that provide PNP SiGe HBTs. We also investigated, for the first time, the feasibility of using inverse-mode SiGe HBTs (emitter and collector terminals swapped) in current mirrors for radiation hardening purposes, because it has

been demonstrated that SiGe HBTs under inverse-mode operation can improve singe-event upset (SEU) sensitivity [42].

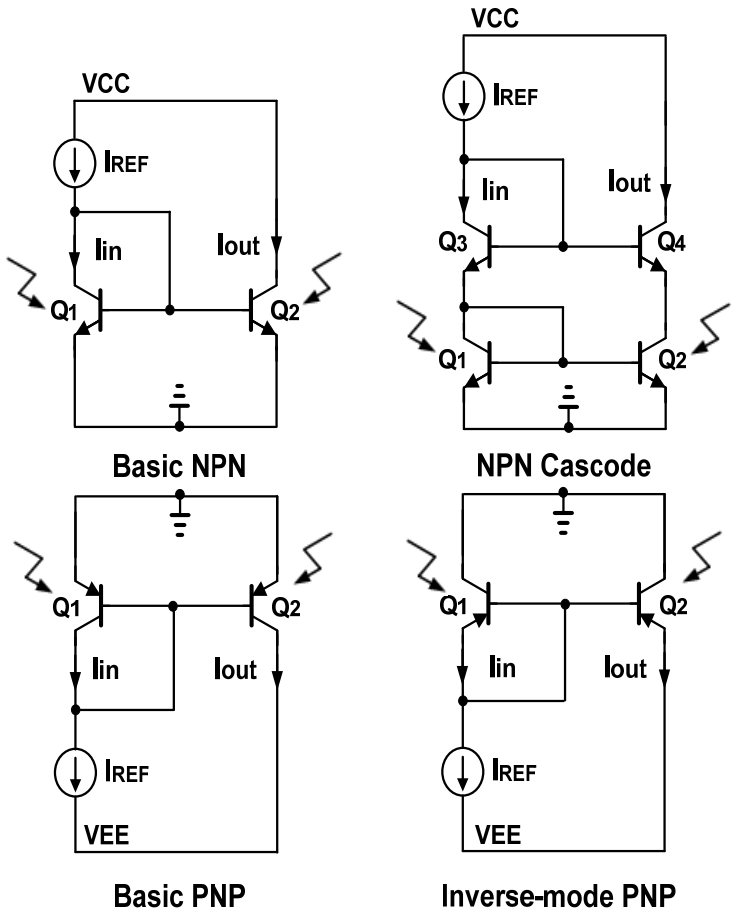


Fig. 4.3: Four types of current mirrors were investigated: basic NPN, cascode NPN, basic PNP, and inverse-mode PNP current mirror.

4.3 Experimental Details

Single-event transient (SET) measurements were performed at the Naval Research Laboratory (NRL) using a two-photon absorption (TPA) pulsed laser system. The system is capable of producing a 1.2 μm diameter charge distribution profile with

automated 3-D positioning and voltage sweeps [45]. The TPA system was configured to produce optical pulses at 1260 nm at a frequency of 1 kHz, with a pulse width of approximately 150 fs. The laser-induced transient waveforms were captured using a high-speed Tektronix DPO71254 12.5 GHz, 50 GS/sec real time oscilloscope. The samples under test were packaged using a high-speed custom-designed printed circuit board using Southwest Microwave SMA end launchers, low loss SMA cables, Keithley 2400 DC power supplies, and bias tee's. The detailed setup is shown in Fig. 4.4. The input and output terminals are connected to both the oscilloscope (channel 1 and 3) and Keithley DC power supplies through RF bias tee's. The emitters are connected to the common-ground node which is shared by all measurement instruments. The channel 2 of the oscilloscope is also connected to the ground node to monitor the AC transients. SETs were measured through the AC input (I_{in}) and output (I_{out}) currents while one of two devices (Q_1 or Q_2) was struck by the laser.

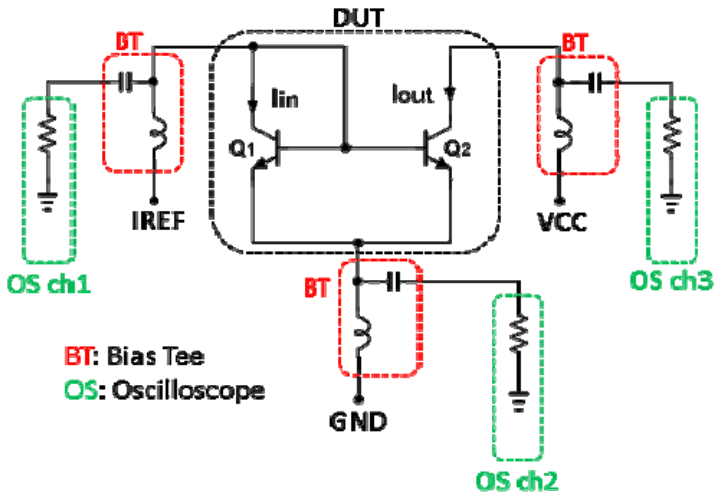


Fig. 4.4: Experimental measurement setup. The samples were mounted on high-speed custom-designed printed circuit board.

4.4 TCAD Modeling

For an in-depth analysis of the complex single-event transient mechanisms in C-SiGe HBTs on SOI, a 3-D model deck was developed for a 0.25 μm x 0.4 μm and 0.25 μm x 1 μm CBC8 NPN and PNP p-cell HBTs, respectively, and full 3-D simulations were employed utilizing CFD Research Corporation's NanoTCAD software package [46]. The models were calibrated for fully-coupled, mixed-mode Spectre simulations by adjusting the TCAD model parameters until the forward-active performance of NanoTCAD model and that of the Spectre compact model closely matched.

The agreement of the forward-active Gummel characteristics of the TCAD and Spectre models is shown in Fig. 4.5. In order to simulate the worst-case scenario of SEU, all subsequent ion-strike locations are fixed at the physical emitter center of both NPN and PNP SiGe HBTs; the ion passes through emitter-base, base-collector, and collector-substrate junctions, which are all sensitive device areas (Fig. 4.6). The simulated electrical collector transient currents of NPN SiGe HBT in forward-active region across multiple ion LETs are shown in Fig. 4.7. The figure can be characterized into two sections of the transient wave form; referred to as section A and B. Section A originates from the collapse of the emitter-base and base-collector depletion regions (collapse of the energy bands) from the large charge carrier influx immediately after the ion-strike, which is known as the "ion-shunt" effect [47]-[48]. The collapse of the reverse-biased collector-base depletion region causes a push-out of the electric field across the narrow base region to the emitter; this decreases the impedance between the collector and emitter terminals. This shunt path allows a large current to flow from separated charges from the ion-strike and the emitter. The free charge carrier concentration drops as the ionized electron-hole pairs are separated and removed from the active area by the electric filed. After the concentration of the ionized carriers drops below the doping level, the base-emitter and base- collector depletion regions re-form. The reform of the electric field marks the beginning of section B; the reestablished electric field in the depletion region of the base-

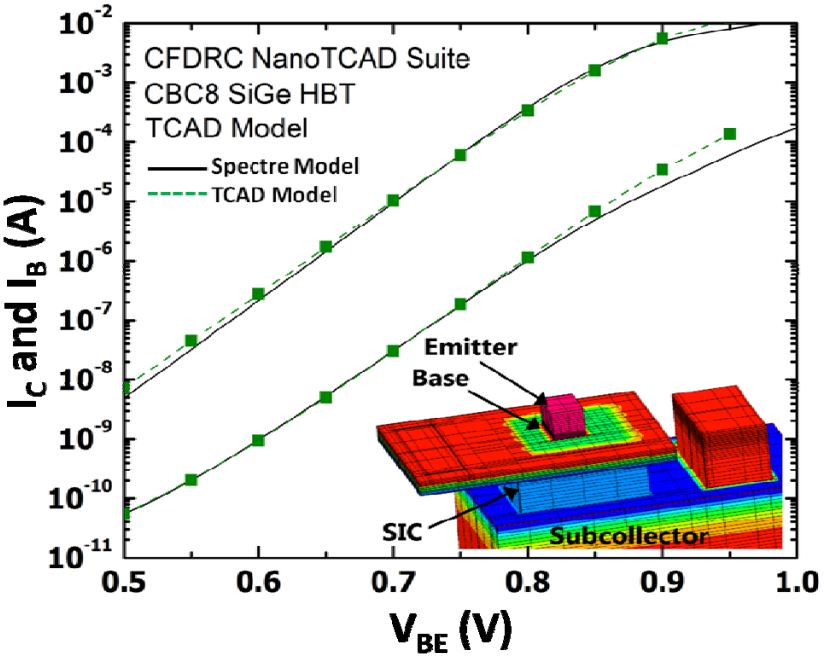


Fig. 4.5: Forward-active Gummel simulation for CBC8 NPN HBT DC calibrated 3-D NanoTCAD model.

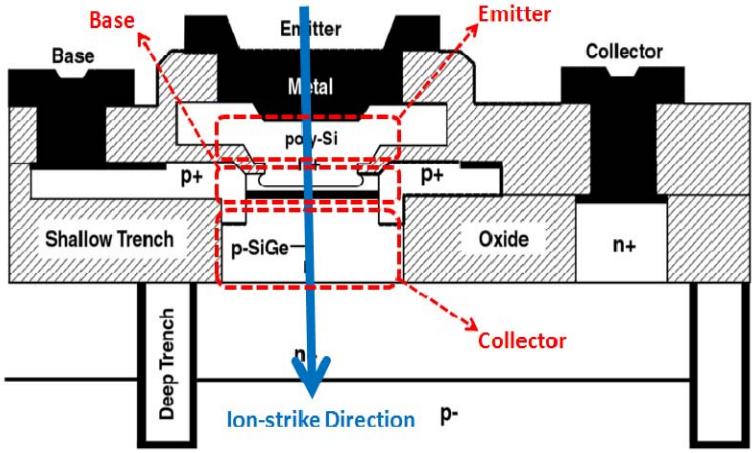


Fig. 4.6: All ion-strike location is fixed at the physical emitter center of HBTs in order to simulate the worst-case scenario of SEU in NanoTCAD device modeling.

emitter and base-collector junctions separates the remaining ion-deposited charges in the SiGe HBT.

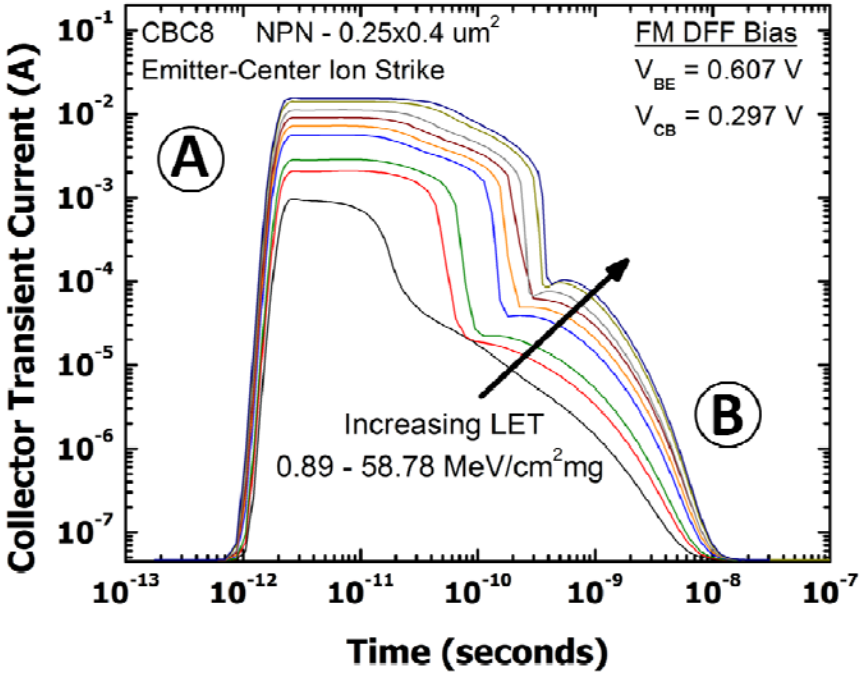


Fig. 4.7: The simulated electrical collector transient current of NPN HBT for forward-active region across multiple ion LETs.

4.5 Basic NPN vs. Cascode NPN Current Mirrors

The basic NPN and cascode NPN current mirrors were irradiated and analyzed with respect to the overall SET sensitivity utilizing NRL's backside laser TPA measurement system. The basic current mirror topology is the most commonly employed current mirror architecture for DC biasing. In some high performance applications, however, the cascode topology is preferred because of its higher output resistance compared to the basic mirror. Understanding the reaction of these two current mirrors

with respect to single events is crucial for designing extreme-environment electronic systems.

The 2-D raster scan in Fig. 4.8 shows the AC output peak transient currents of Q_2 and Q_4 of the basic NPN and cascode NPN current mirrors as the input SiGe HBTs (Q_1s) are struck by the laser with an energy of 10 pJ. The most noticeable observation is that the transient currents are well confined inside the deep trench (DT) isolation box (yellow dotted line), as expected for both the basic NPN and cascode NPN current mirrors. Unlike SiGe HBTs in non-SOI (bulk) platforms, SiGe HBTs in SOI processes are protected against ion-strike induced transient currents from adjacent SiGe HBTs since they are isolated by the DT isolation and SOI buried layer (Fig. 4.9). This implies that the transient currents can affect other SiGe HBTs only through metal line connections (not through the substrate). The area of charge generation for the cascode NPN current mirror is broader than that of the basic NPN current mirror due to the AC transient charge circulation both at the base and the emitter of the output SiGe HBT (Q_4) through Q_2 and Q_3, while the transient charge circulation is experienced only by the base of the output SiGe HBT Q2 in the basic NPN mirror because the emitter is tied to the ground.

The collector of the common-emitter transistor Q_2 is connected to the emitter of the output SiGe HBT Q_4 in the cascode NPN current mirror. This produces a positive feedback seen looking into the output terminal of Q_4, increasing the output resistance of the cascode current mirror. This positive feedback is reflected in the denominator of the output resistance equation (2), where r_{o2} and r_{o4} are the output resistance of Q_2 and Q_4, respectively, r_{ie4} is the *Thevenin* equivalent resistance seen looking into the emitter of Q_4, and α_4 is the common-base current gain of Q_4.

$$r_{out\_cascode} = \frac{r_{o4} + r_{ie4} \parallel r_{o2}}{1 - \dfrac{\alpha_4 r_{o2}}{r_{ie4} + r_{o2}}} \qquad (2)$$

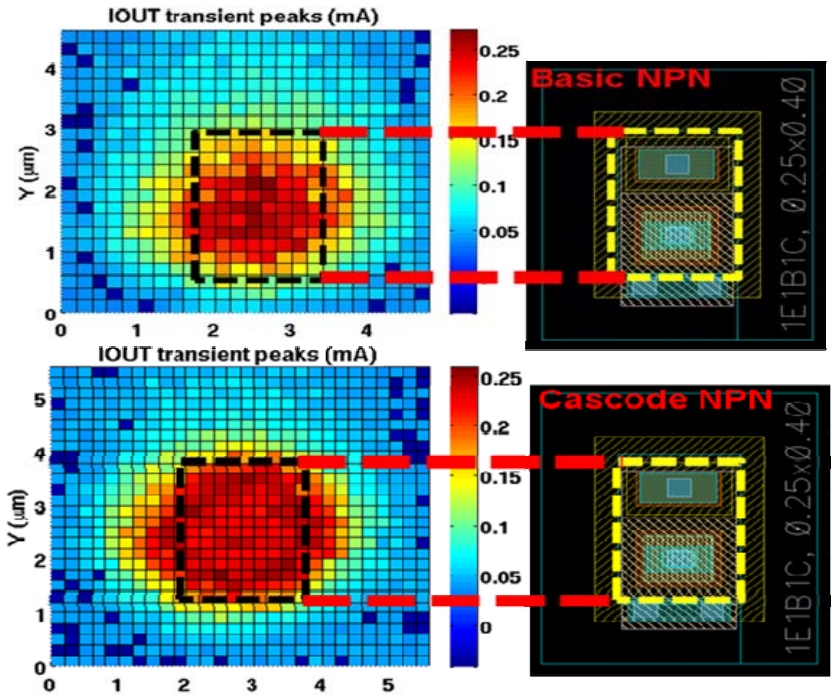


Fig. 4.8: 2-D raster scan shows the AC output peak transient currents of Q_2 and Q_4 of the basic NPN and cascode NPN current mirrors as the input SiGe HBTs (Q_1s) are struck by the laser of 10 pJ.

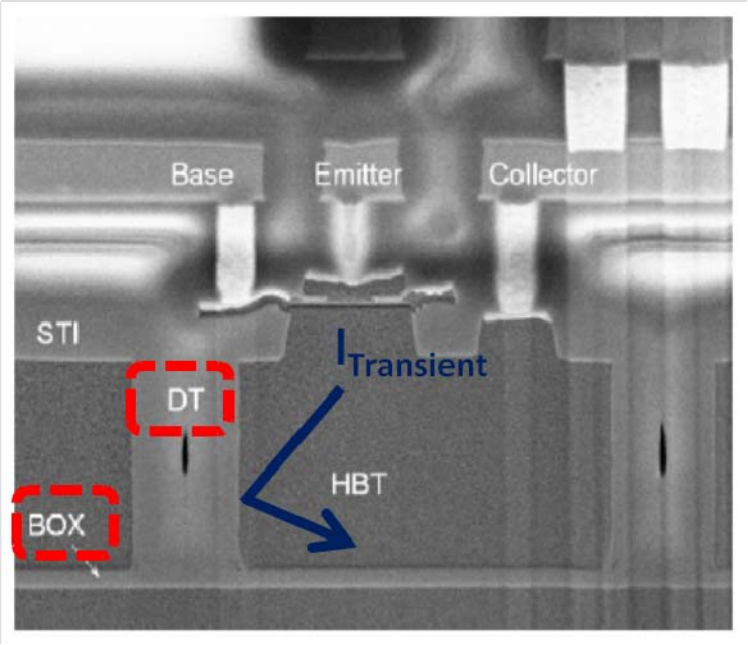


Fig. 4.9: The ion-strike induced AC transient currents are well confined inside the deep trench (DT) isolation and SOI box.

As a result, the settling time of the output transient current in the cascode current mirror is longer than that of the basic NPN current mirror, as the Q_1s are impacted by the laser-strike (ΔS in the upper plot of Fig. 4.10); i.e., the time constant of the cascode ($\tau_{cascode} = R_{cascode}C_{cascode}$) is greater than that of the basic NPN ($\tau_{basicNPN} = R_{basicNPN}C_{basicNPN}$) current mirror. The transient peaks of the input current are relatively small both in the basic NPN and cascode NPN current mirrors due to the diode connection as Q_2s are struck by the laser (lower plot of Fig. 4.10). The diode connection in Q_1s provides a shunt-shunt negative feedback and lessens the SET impact.

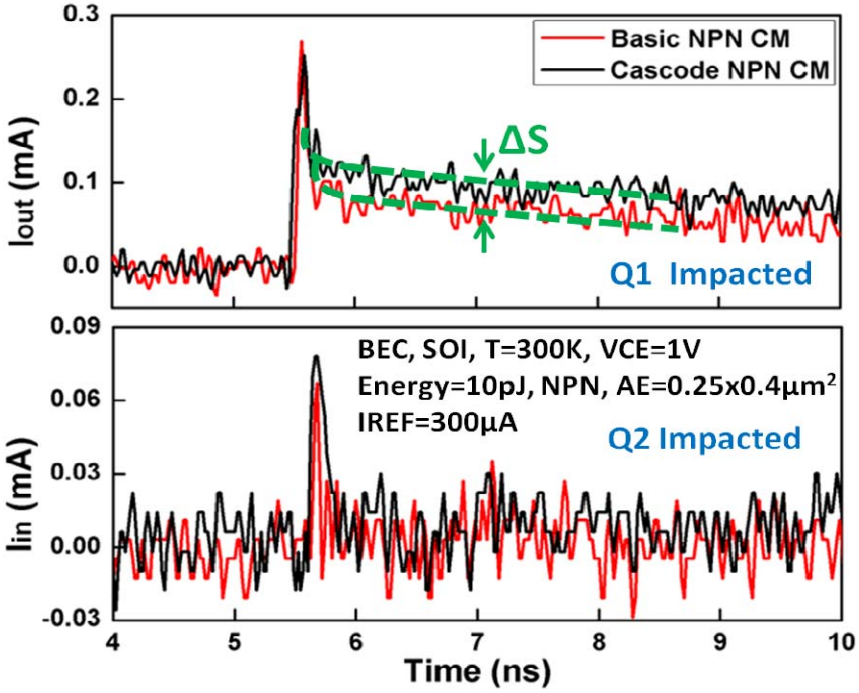


Fig. 4.10: The settling time of the output transient current in the cascode current mirror is longer than that of the basic NPN current mirror when the input device Q_1s are impacted (struck by the laser). The laser-strike effects on the input current are relatively small when the output SiGe HBTs (Q_2s) are impacted due to the diode connection in Q_1s that provides a negative feedback.

The single-event induced peak input (I_{in}) and output (I_{out}) transient currents over the width (x-direction in Fig. 4.8) of Q_1 and Q_2 across the most sensitive region in the basic NPN and cascode NPN current mirrors are shown in Fig. 4.11. Relatively large peak transients in both I_{in} and I_{out} can be observed as Q_1s in the current mirrors experience the strike along the width. However, when Q_2s are struck by the laser, only the output current (I_{out}) experiences significant transients, while the transients in the input current are small because of the negative feedback provided by the diode connection in $Q1_s$.

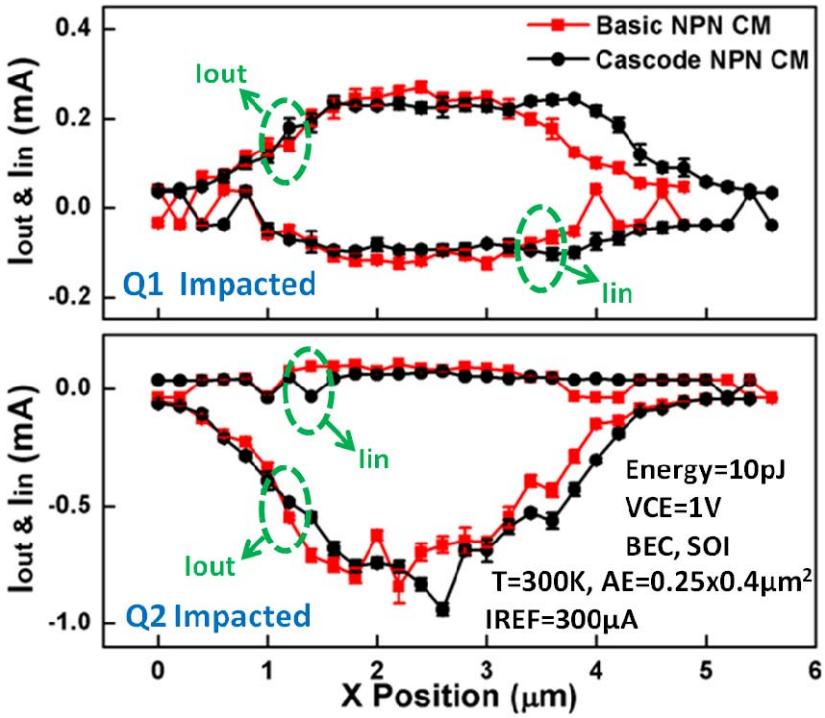


Fig. 4.11: The single-event induced peak transient input and output currents over the width (x-direction in Fig. 4.8) of Q_1 and Q_2 across the most sensitive region in the basic NPN and cascode NPN current mirrors.

4.6 Basic NPN vs. Basic PNP Current Mirrors

In order to understand the complex single-event transient mechanisms of C-SiGe NPN and PNP HBTs on SOI, a 3-D model deck was developed and used in mixed-mode TCAD simulations using Cadence. The reference current I_{REF} was chosen such that the current density of the two current mirrors was 1.5 mA/μm^2.

Fig. 4.12 and 4.13 show the mixed-mode simulation results of the input (I_{in}), output (I_{out}), and ground (I_{gnd}) transient currents both in the basic NPN and basic PNP current mirrors as the input device Q_1 (Fig. 4.12) and the output device Q_2 (Fig. 4.13) are impacted by the laser strike, respectively. The basic PNP current mirror clearly exhibits the higher radiation tolerance compared to the basic NPN current mirror against the strike.

The measured results validate the mixed-mode TCAD simulations. The 2-D raster scan in Fig. 4.14 shows the AC output peak transient currents of Q_2s in the basic NPN and basic PNP current mirrors as the input SiGe HBTs (Q_1s) are struck by the laser of 10 pJ. As with the SiGe NPN HBT on SOI current mirror, the transient currents are well confined inside the deep trench (DT) isolation and SOI box in the SiGe PNP HBT on SOI current mirror. The magnitude of the output peak transient current of the basic PNP current mirror is less than that of the basic NPN mirror, as shown in Fig. 4.14 and 4.15. According to Fig 4.15, the basic PNP current mirror exhibits a shorter settling time (ΔS in Fig. 4.15). The strike induced input peak transient currents (I_{in}) are relatively small in both the basic NPN and PNP current mirrors because of the negative feedback produced by the diode connection in Q_1s. The single-event induced peak input (I_{in}) and output (I_{out}) transient currents over the width (x-direction in Fig. 4.14) of Q_1 and Q_2 across the most sensitive region in the basic NPN and basic PNP current mirrors are shown in Fig. 4.16. It can be observed in the figure that the output transient current of the basic PNP current mirror is smaller than that of the basic NPN current mirror when Q1 and Q2 are struck by the laser over the width. The input transient current of the basic PNP current mirror is

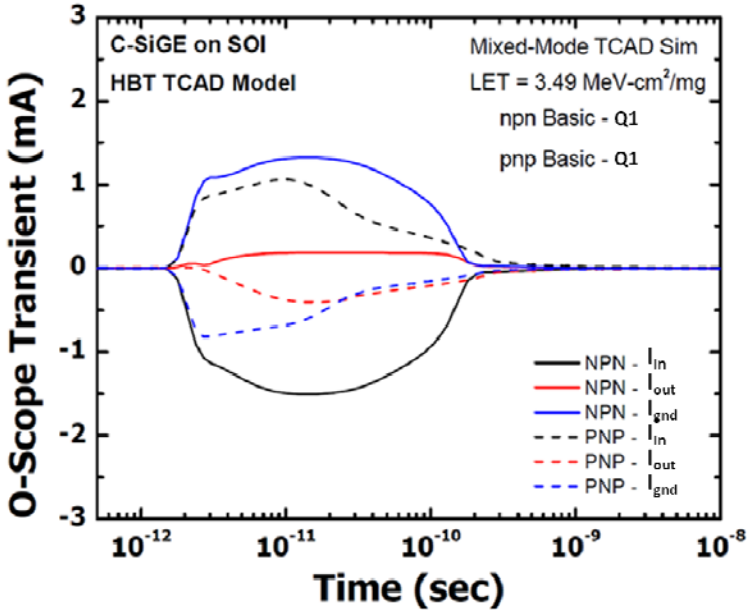


Fig. 4.12: Mixed-mode simulation results of the ion-strike induced transient currents in the basic NPN and basic PNP current mirrors as the input device Q_1s are impacted by the laser.

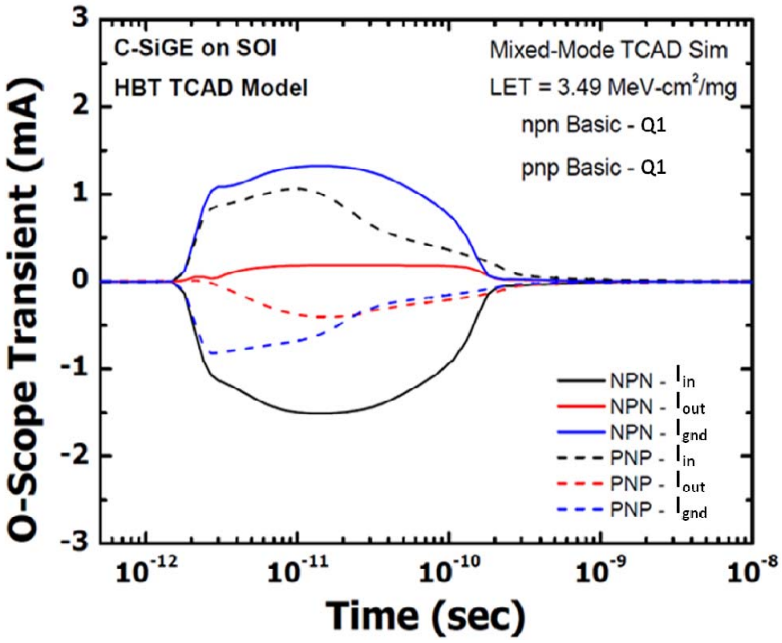


Fig. 4.13: Mixed-mode simulation results of the ion-strike induced transient currents in the basic NPN and basic PNP current mirrors as the output device Q_2s are impacted by the laser.

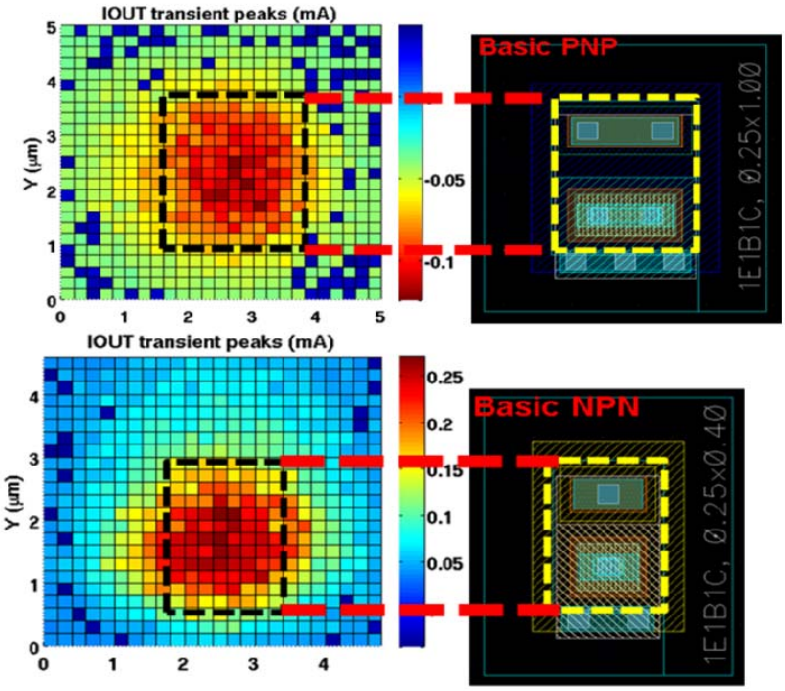


Fig. 4.14: 2-D raster scan shows the AC output peak transient currents of Q_2s as the input SiGe HBTs (Q_1s) are impacted by the laser of 10 pJ in the basic NPN and basic PNP current mirrors.

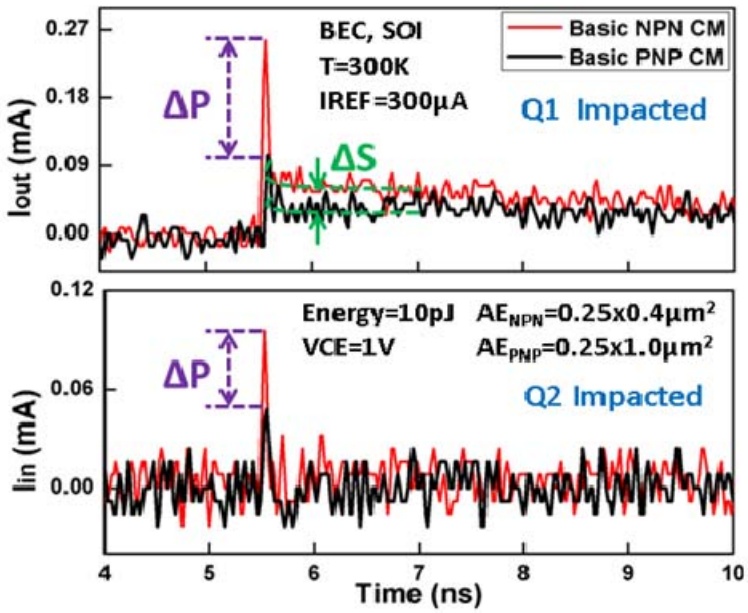


Fig. 4.15: The settling time of the output transient current in the basic PNP current mirror is shorter than that of the basic NPN current mirror when the input device Q_1s are impacted.

also smaller than that of the basic NPN current mirror when Q_1 is impacted; however, due to the diode connection, when Q_2 is struck by the laser, the difference between the input transient currents is minimal.

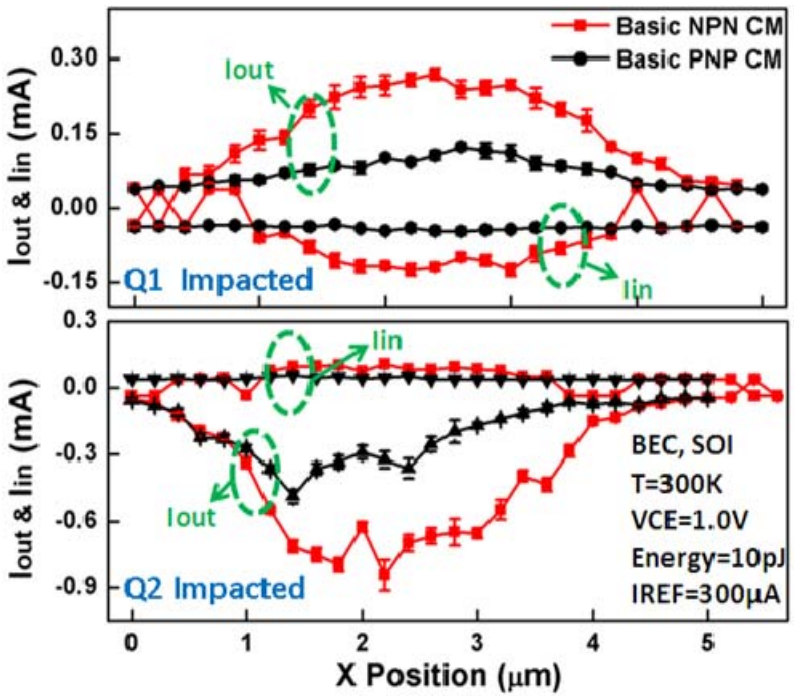


Fig. 4.16: The single-event induced peak transient input and output currents over the width (x-direction in Fig. 4.14) of Q_1 and Q_2 across the most sensitive region in the basic NPN and basic PNP current mirrors.

4.7 Inverse-Mode PNP Current Mirror

The inverse-mode of operation has often been viewed as a non-viable mode of operation because it suffers from poor DC and AC performance. However, it has been experimentally demonstrated that SiGe HBTs can be utilized and optimized for the inverse-mode operation [49]. We also investigated the feasibility of utilizing inverse-mode PNP SiGe HBTs in current mirrors for the radiation hardening purposes. The

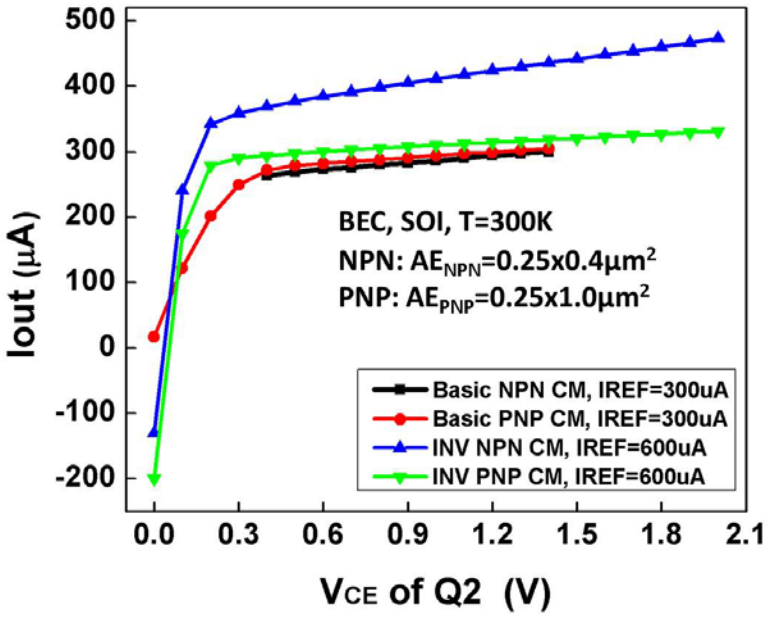


Fig. 4.17: Preliminary DC measurement validates that the inverse-mode SiGe PNP HBTs can be used in current mirrors. The electrical collector (physical emitter) current curve is as flat as those of the basic NPN and PNP current mirrors over the collector-emitter voltage V_{CE}.

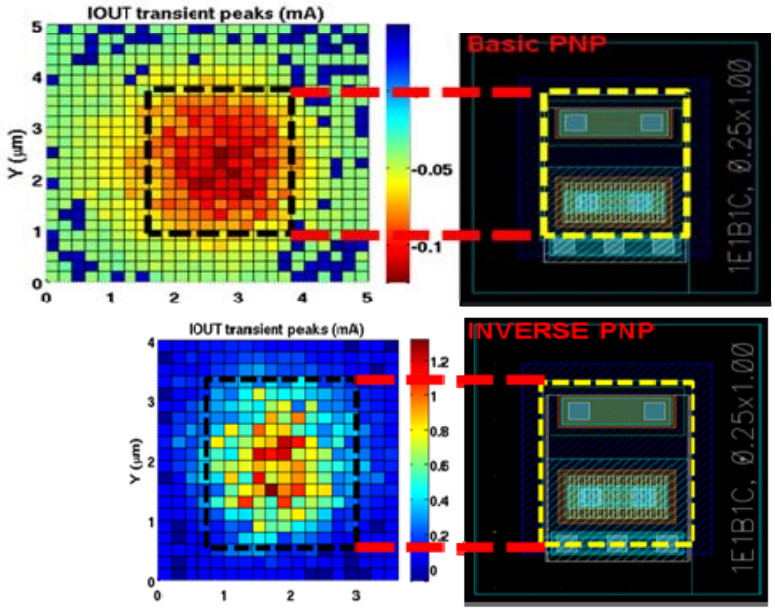


Fig. 4.18: 2-D raster scan shows the AC output peak transient currents of Q_2s as the input SiGe HBTs (Q_1s) are impacted by the laser in the basic PNP and inverse-mode PNP current mirrors. The basic PNP and inverse-mode PNP current mirrors were irradiated at 10 pJ and 66 pJ, respectively.

preliminary measurement results on the inverse-mode PNP current mirror in Fig. 4.17 validate that the inverse-mode CBC-8 C-SiGe PNP HBTs can be used in current mirrors. The electrical collector (physical emitter) current curve is nearly as flat as those of the basic NPN and PNP current mirrors over a wide range of the collector-emitter voltage V_{CE}; in low V_{CE} region, the inverse-mode current mirrors exhibit even flatter I_{out} curve than the forward-mode mirrors because of their lower knee voltage.

Fig. 4.17 also shows that the inverse-mode SiGe PNP HBTs can implement more ideal current mirrors than the inverse-mode SiGe NPN HBTs, since the slope of the output current curve is lower than that of the inverse-mode SiGe NPN HBT. There is, however, an apparent drawback in utilizing the inverse-mode SiGe HBTs in current mirrors: the discrepancy between the reference current and the mirrored current. However, this discrepancy can be corrected for by choosing a larger output device size or connecting small output devices in parallel.

The inverse-mode PNP current mirror was irradiated at more than a 6x higher energy level (66 pJ) than the forward-mode current mirrors. The comparison between 2-D raster scans of the basic PNP and inverse-mode PNP current mirrors in Fig. 4.18 clearly demonstrates the excellent radiation tolerance of the inverse-mode PNP current mirror against the laser strikes; the magnitude of the peak transient current is lower and the region of impact is smaller than those of the basic PNP current mirror. Also note that the transient currents are well confined by DT isolation and SOI, as with the forward-mode current mirrors.

4.8 Summary and Implications

This work has investigated the single-event transient (SET) response of various current mirrors (a fundamental DC bias block for both analog and RF circuits), all implemented in C-SiGe HBT on SOI technology. We have also addressed the feasibility

of employing the inverse-mode SiGe HBTs in current mirrors to lessen the single-event effects. Based on the measurement results and TCAD analysis presented, some practical suggestions and observations can be made for operation of such current mirrors in extreme-environments.

First, the basic NPN current mirror is recommended over the cascode NPN current mirror because it has higher SET tolerance than the cascode NPN current mirror in terms of the lower peak transient, shorter settling time, and smaller area of impact across the HBTs. However, if higher impedance is required at the output terminal, the cascode current mirror is recommended.

Second, utilizing PNP SiGe HBTs instead of NPN SiGe HBTs in current mirrors can make the AC transients of the input and output currents (induced by the laser (ion) strike) shorter and their peaks smaller. The inverse-mode PNP current mirror was capable of mirroring the reference current to the output terminal with mirror-ratio corrections. It also could supply a constant current over a wide range of the collector-emitter voltage V_{CE} of the output SiGe HBT (wider than that of forward-mode current mirrors). The measurement results also showed the excellent SET tolerance of the inverse-mode PNP current mirrors. The SET effects were not significant compared to those of the forward-mode basic NPN, cascode NPN, and basic PNP current mirrors; even at an elevated energy level (more than 6x), the inverse-mode PNP current mirror exhibited lower peak transient output current than the basic PNP current mirror.

4.9 Acknowledgement

This work was supported by the Defense Threat Reduction Agency under contract HDTRA1-13-C-0058. Seungwoo Jung would like to graciously thank Texas Instruments for access to their CBC-8 C-SiGe HBT on SOI process.

CHAPTER 5

GAIN-BANDWIDTH IMPROVEMENT TECHNIQUES IN TRANSIMPEDANCE AMPLIFIERS FOR OPTICAL COMMUNICATIONS

5.1 Introduction

This work demonstrates techniques for attaining wide bandwidth and high gain in transimpedance amplifiers (TIAs) intended for optical communications by reducing input impedance and causing gain-bandwidth product to be non-constant. The major obstacle to achieving wide bandwidth and high gain in a TIA is a dominant pole caused by the large parasitic capacitance associated with the input photo-diode. The proposed TIA architecture employs a common-base differential pair at the input and global (as opposed to local) feedback to overcome this challenge. A signal flow graph approach is utilized to perform a detailed ac analysis of the circuits.

Three circuits were fabricated utilizing complementary silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) on Silicon on insulator (SOI) technology. Measured results indicate the proposed TIA can achieve a non-constant gain-bandwidth product; that is, increasing both gain and bandwidth while only slightly degrading noise performance.

The major challenge to achieve a wide bandwidth and high gain in transimpedance amplifier (TIA) design is the dominant pole induced by the large parasitic capacitance associated with the input photo-diode. The capacitance values of the photo-diode can be up to several pF [50]. This capacitance, together with the input impedance of a TIA, sets the cut-off frequency determining the bandwidth (1). Fig. 5.1

illustrates a differential TIA with an input impedance of *Rin* connected to a photo-diode capacitance $C_{PhotoDiode}$.

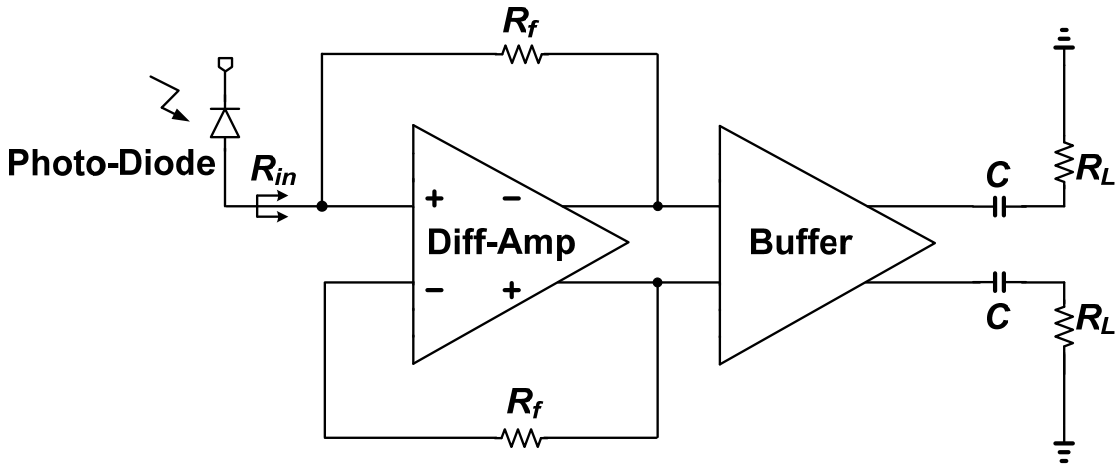


Fig. 5.1: Differential transimpedance amplifier (TIA) with an input photo-diode. The input impedance of the TIA is denoted as R_{in}.

Conventional TIAs employ a common-emitter differential pair as their input stage [51]-[52]. However, this can limit the bandwidth when the input capacitance is large because the impedance seen looking into the bases of a common-emitter differential pair is large as well. Since the input capacitance is intrinsic to a photo-diode and thus unalterable, the input impedance of a TIA must be reduced significantly to expand the bandwidth (eqn. (1)).

$$\omega_{cut\_off} = \frac{1}{R_{in} C_{PhotoDiode}} \tag{1}$$

As a solution to this problem, previous authors have cascaded a common-base amplifier before a common-emitter main gain stage [53]-[54].

The design presented in this work exploits a common-base differential amplifier as an input stage to reduce the input impedance. However, unlike in other published work, it employs global (as opposed to local) feedback to cause the gain-bandwidth product to be non-constant. The feedback networks in other designs are connected between their output and the input of a common-emitter amplifier, which is the main gain stage, instead of a common-base amplifier. Another advantage of global feedback is that it reduces the input impedance further, by the amount of feedback ($1+A_{OL}\beta_f$), by forming a shunt feedback at the input side. The non-constant gain-bandwidth product is produced by increasing the open-loop gain as well as the transimpedance gain (approximately, the feedback resistance) simultaneously [4]. This concept is elaborated in detail in section 5.3.

Signal flow graphs are used for the ac analysis of the proposed TIA, as they have been proven to be advantageous in analyzing systems and circuits containing feedback networks [19]-[20], [55]. Three circuits were fabricated on a silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) on Silicon on insulator (SOI) technology with a peak f_T of 50 GHz ([8], [15], [56]) and measured to verify the non-constant gain-bandwidth product of the proposed TIA, as well as to compare the noise performance between the conventional and proposed TIAs at the same gain. The parasitic input capacitance is 2 pF.

5.2 TIA Architecture and AC Analysis

The following notations are used throughout the paper. The *Thevenin* equivalent voltage and resistance seen looking into a node are denoted with subscripts starting with *i* and seen looking out of a node are denoted with subscripts starting with *t*. Table I shows some examples.

Table 5.1: Notation Examples.

Example	*Interpretation*
V_{ia}	*Thevenin* voltage seen looking into node a
R_{ia}	*Thevenin* resistance seen looking into node a
V_{ta}	*Thevenin* voltage seen looking out of node a
R_{ta}	*Thevenin* resistance seen looking out of node a

Figure 5.2 shows a conventional differential TIA with a common-emitter differential input pair. With the feedback loop removed, the input resistance seen looking into the base of Q3 of the TIA is given by

$$r_{in\_conv} = \left[r_{\pi 3} + r_x + (1+\beta_3)R_{te3}\right] \| R_5 \| R_7 \tag{2}$$

where r_x is the base spreading resistance, and R_{te3} is the *Thevenin* equivalent resistance seen looking out of the emitter of Q3.

The proposed TIA architecture is illustrated in Fig. 5.3. A common-base differential pair Q13 and Q14 (circled with the dotted line) are cascaded prior to the common-emitter differential input stage. A global feedback network is connected from the output to the emitters of the common-base differential pair, as oppose to the typical local feedback connecting to the bases of the common-emitter pair (Q3 and Q4). TIAs utilizing a common-base stage to reduce the input impedance have been previously

designed, but their feedback networks were connected to the base of the common-emitter stages (local feedback) [53]-[54]. The global feedback network with the common-base

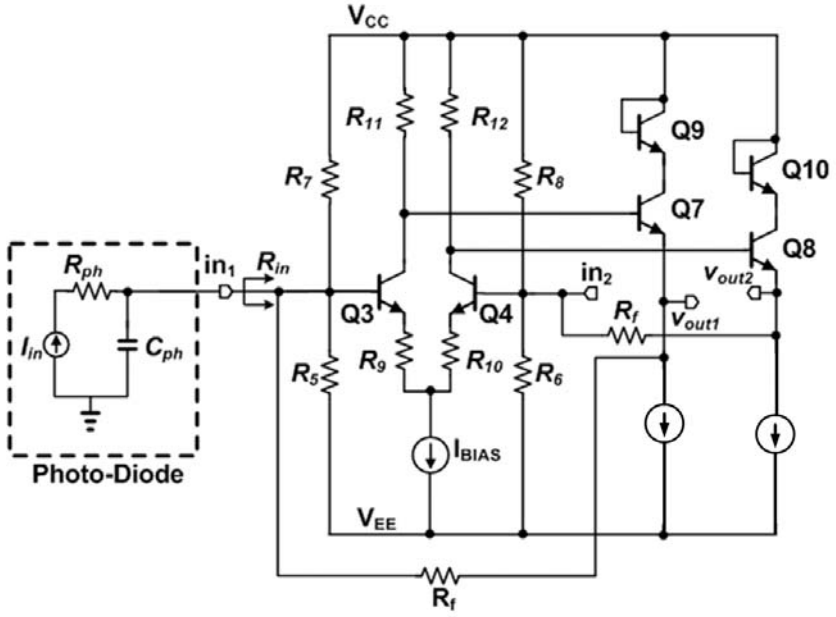


Fig. 5.2: Conventional differential TIA with a common-emitter differential input stage. Parasitic photo-diode capacitance is denoted as C_{ph}.

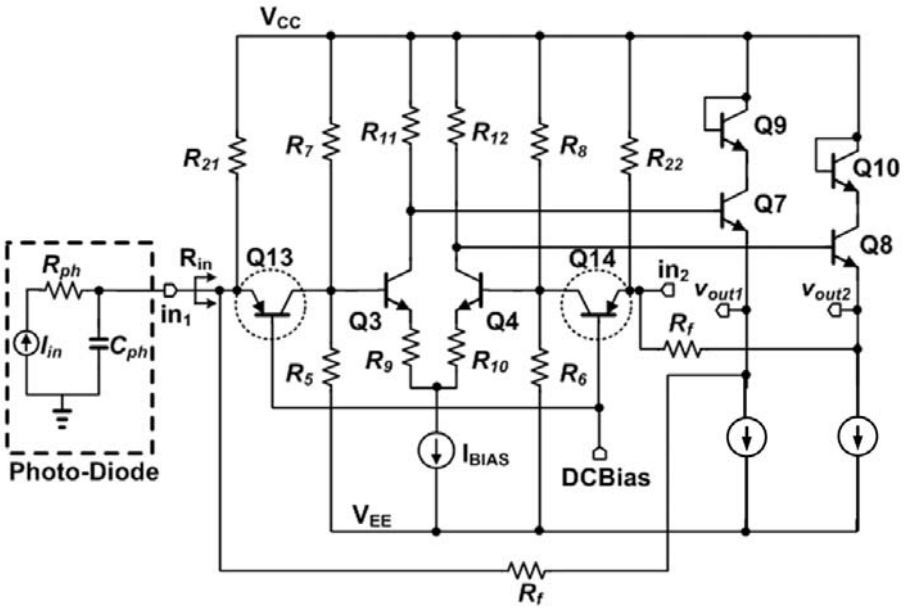


Fig. 5.3: Proposed differential TIA with a common-base differential pair input stage and a global feedback. Parasitic photo-diode capacitance is denoted as C_{ph}.

differential pair further reduces the input impedance by the amount of feedback ($1+A_{OL}\beta_f$) because shunt feedback is created at the input. In addition, it causes the gain-bandwidth product of the amplifier to be non-constant by causing the open-loop gain to change as the feedback resistance varies.

The feedback loops of the proposed TIA are removed for the ac-analysis in Fig. 5.4. The circuit seen looking into the feedback network at the emitter of Q13 is replaced with a *Norton* equivalent circuit with respect to v_{out1}, and the circuit seen looking into the feedback network at the emitter node of Q7 is replaced with a *Thevenin* equivalent circuit with respect to the emitter voltage v_{e13} of Q13. The same procedure is taken at the emitter node of Q14 and the emitter node of Q8 to remove the other feedback loop. Since the negative feedback network has the effect of making the current smaller at the input node (i.e. the error current becomes smaller) to the level at which its effect on the overall gain is negligible, the feed-forward gains by v_{e13} and v_{e14} (represented as dependent sources at the differential output in the figure) are ignored.

The signal flow graph in Fig. 5.5 is constructed based on the circuit schematic in Fig. 5.4. The determinant can be calculated from the signal flow graph as ([19]-[20])

$$\Delta = 1 - \left[g_{m13} R_{tb3} G_{mdiff} (-R_{11}) K \frac{R_{e13}}{R_f} + R_{12} K \frac{R_{e13}}{R_f} g_{m14} R_{tb3} (-G_{mdiff}) \right] \tag{3}$$

where *Gmdiff* and *Rtb3* are the effective transconductance of common-emitter pair (Q3 and Q4) and the *Thevenin* equivalent resistance seen looking out of the base of Q3, respectively.

$$G_{mdiff} = \frac{1}{r_{ie3} + r_{ie4} + R_9 + R_{10}} \tag{4}$$

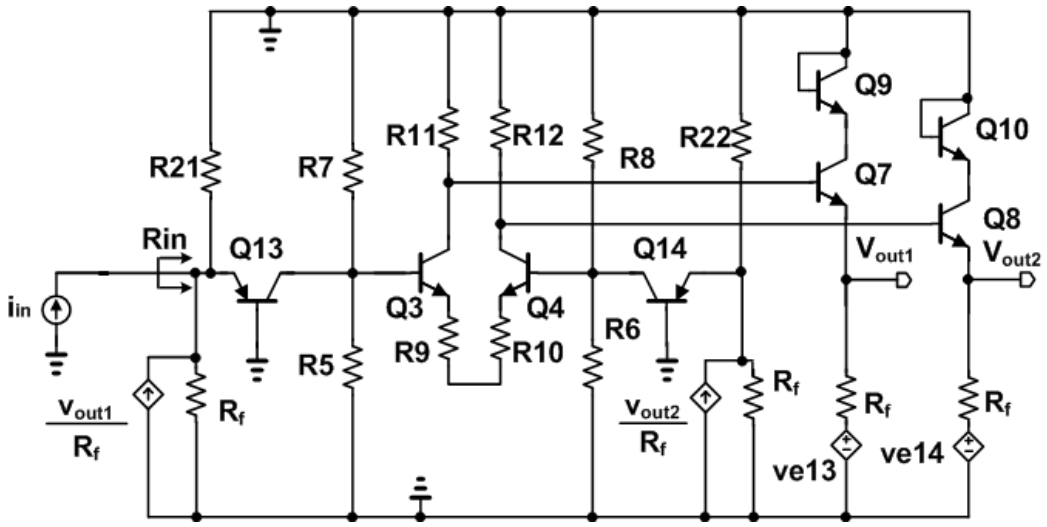


Fig. 5.4: The proposed TIA with the feedback network removed for the ac analysis. All dc voltage sources are grounded and current sources are open circuited. The feedback network is replaced with the *Thevenin* and *Norton* equivalents.

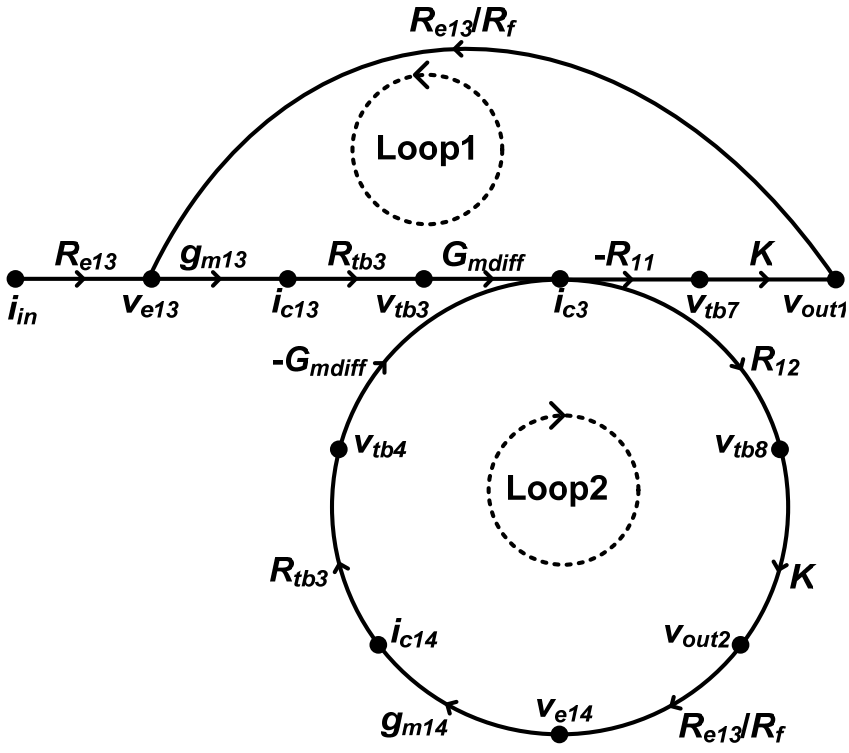


Fig. 5.5: Signal flow graph for the ac analysis of the proposed TIA.

$$R_{tb3} = R_5 \parallel R_7 = R_{tb4} = R_6 \parallel R_8 \tag{5}$$

The *Thevenin* equivalent resistance seen looking into the emitter of Q3 and Q4 are denoted as *rie3* and *rie4* in (4), and their values are

$$r_{ie3} = \frac{1}{g_{m3}} + \frac{R_{tb3}}{1+\beta_3} = r_{ie4} = \frac{1}{g_{m4}} + \frac{R_{tb4}}{1+\beta_4} \tag{6}$$

K is defined as

$$K = \frac{R_f}{r_{ie7} + R_f} = \frac{R_f}{r_{ie8} + R_f} \tag{7}$$

where *rie7* and *rie8* are the *Thevenin* equivalent resistances seen looking into the emitters of Q7 and Q8. R_{e13} is given by

$$R_{e13} = R_f \parallel R_{21} \parallel \frac{1}{g_{m13}} = R_{e14} = R_f \parallel R_{22} \parallel \frac{1}{g_{m14}} \tag{8}$$

Since the architecture of the TIA is symmetrical, the determinant in (3) can be rewritten as

$$\Delta = 1 + 2g_{m13}R_{tb3}G_{mdiff}R_{11}K\frac{R_{e13}}{R_f} \tag{9}$$

By an inspection of the signal flow graph, the differential transimpedance gain can be attained as ([19]-[20])

$$\frac{v_{diff}}{i_{in}} = \frac{-2R_{e13}g_{m13}R_{tb3}G_{mdiff}R_{11}K}{1+2R_{e13}g_{m13}R_{tb3}G_{mdiff}R_{11}K(R_f)^{-1}} \tag{10}$$

Equation (10) is of the form

$$\frac{A_{OL}}{1+A_{OL}\beta_f} \tag{11}$$

where

$$A_{OL} = -2R_{e13}g_{m13}R_{tb3}G_{mdiff}R_{11}K \tag{12}$$

$$\beta_f = \frac{1}{R_f} \tag{13}$$

The input impedance can be calculated from the flow graph as

$$R_{in} = \frac{v_{e13}}{i_{in}} = \frac{1}{1-LG_1}R_{e13} \tag{14}$$

LG_1 is the loop-gain of the Loop1 in Fig. 5.5, which is given by

$$LG_1 = -g_{m13}R_{e13}G_{mdiff}R_{11}K\frac{R_{tb3}}{R_f} \tag{15}$$

The dominant pole frequency is determined by the parasitic photo-diode capacitance and the input impedance of a TIA as illustrated in section 5.1. Thus the input

impedance and capacitance need to be reduced to expand the bandwidth. However, since the input capacitance of a photo-diode is fixed, the input impedance must be reduced significantly to expand the bandwidth. The input impedance of the conventional (Fig. 5.2) and the proposed (Fig. 5.3) TIAs with the feedback networks removed are expressed in (2) and (8), respectively. As shown in the equations, the open-loop input impedance of the proposed TIA is smaller than that of the conventional TIA because the impedance seen looking into the emitter of Q13 ($1/g_{m13}$) is much less than the impedance seen looking into the base of Q3 ($r_\pi + r_x + (1+\beta_3)R_{te3}$).

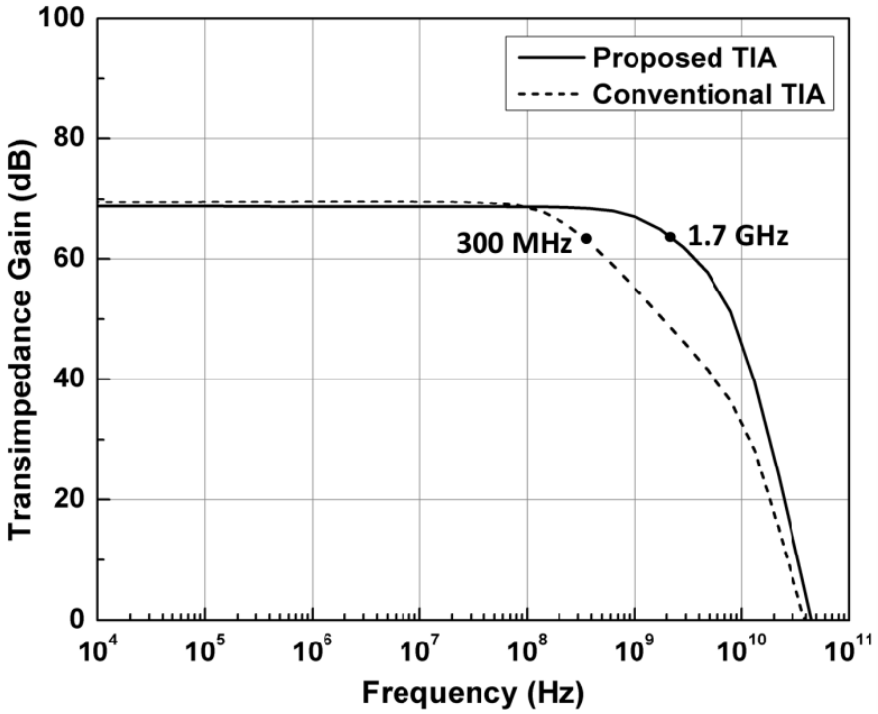


Fig. 5. 6: Simulated frequency response of the conventional TIA (Fig. 5. 2) and the proposed TIA (Fig. 5.3) at the same transimpedance gain. The parasitic photo-diode capacitance is 2 pF.

In addition, the input impedance of the proposed TIA is reduced further by the amount of feedback (1-LG_1), as shown in (14), due to the global feedback compared to that of TIAs employing a common-base input stage with a local feedback; the global feedback returns to the emitter of the common-base stage from the output, while the local feedback returns to the base of the common-emitter stage. The global feedback creates a shunt-summing (i.e., current summing) network at the input of the TIA. Hence, the input impedance is further reduced by the amount of feedback 1-LG_1.

Fig. 5.6 shows the simulated frequency response of the proposed TIA versus the conventional TIA at the same transimpedance gain. The cut-off frequency of the proposed TIA is more than 5 times greater than that of the conventional TIA owing to the very small input impedance as well as the global feedback employed.

5.3 Non-Constant Gain-Bandwidth

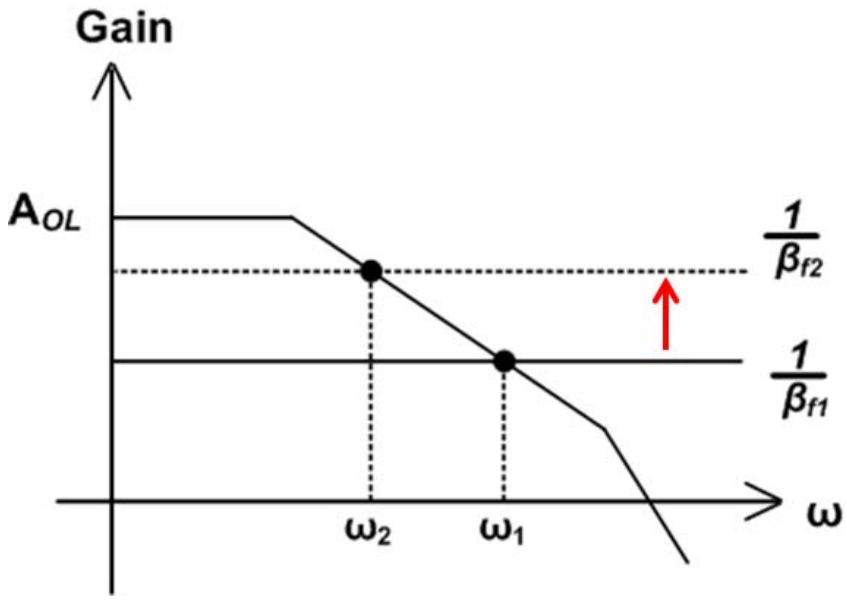


Fig. 5.7: Asymptotic Bode plots of the open-loop gain (A_{OL}) and $1/\beta_f$ whose reciprocal value is approximately the closed-loop gain to illustrate a constant gain-bandwidth product. β_f is a feedback factor, and $\beta_{f1} > \beta_{f2}$.

Fig. 5.7 illustrates the concept of the constant gain-bandwidth product [57]. The gain-bandwidth product is constant when the open-loop gain (A_{OL}) remains the same as the closed-loop gain ($1/\beta_{f1}$ to $1/\beta_{f2}$) varies, as shown in the figure. β_{f1} and β_{f2} are feedback factors whose reciprocal values are approximately the closed-loop gain. For example, the bandwidth decreases (from ω_1 to ω_2) as the gain increases (from $1/\beta_{f1}$ to $1/\beta_{f2}$) maintaining a constant gain-bandwidth product, as can be seen in Fig. 5.7.

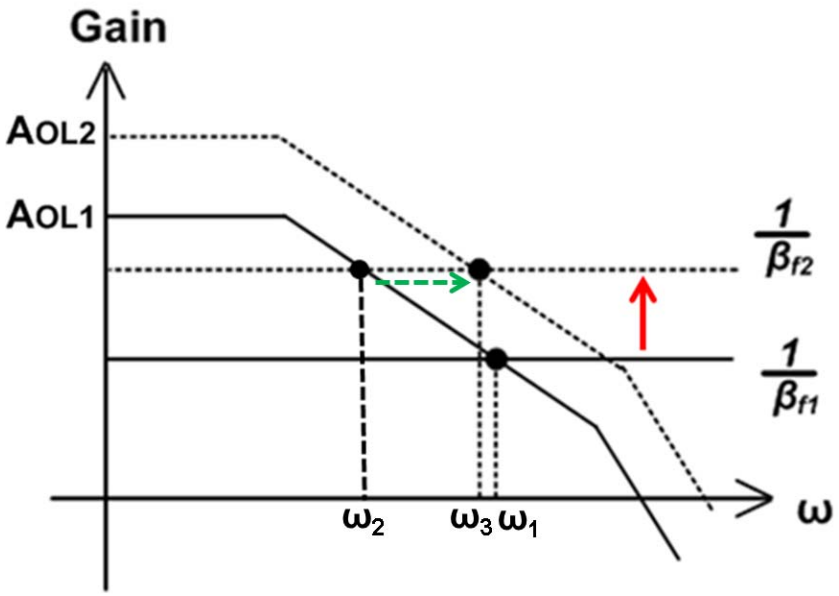


Fig. 5.8: Asymptotic Bode plots of open-loop gain (A_{OL}) and $1/\beta_f$ whose reciprocal value is approximately the closed-loop gain to illustrate a non-constant gain-bandwidth product. β_f is a feedback factor, and $\beta_{f1} > \beta_{f2}$.

The open-loop gain of the proposed TIA in (12) can be simplified by keeping only the terms that contain the feedback resistor R_f as

$$A_{OL}^{*} = g_{m13}R_{e13} = g_{m13}\left(R_f \,||\, R_{21} \,||\, \frac{1}{g_{m13}} \right) = \frac{g_{m13}R_{21}}{g_{m13}R_{21} + 1 + \frac{R_{21}}{R_f}} \tag{16}$$

Equation (16) clearly shows that the open-loop gain of the proposed TIA is affected by the value of the feedback resistor R_f. For example, if the feedback resistance increases, the transimpedance gain increases, but the open-loop gain rises as well, resulting in an increase in the cut-off frequency from ω_2 to ω_3, as shown in Fig. 5.8. This produces the desired non-constant gain-bandwidth product. The simulated frequency response of the proposed TIA with three different feedback resistances (5, 8, 11 kΩ) is shown in Fig. 5.9.

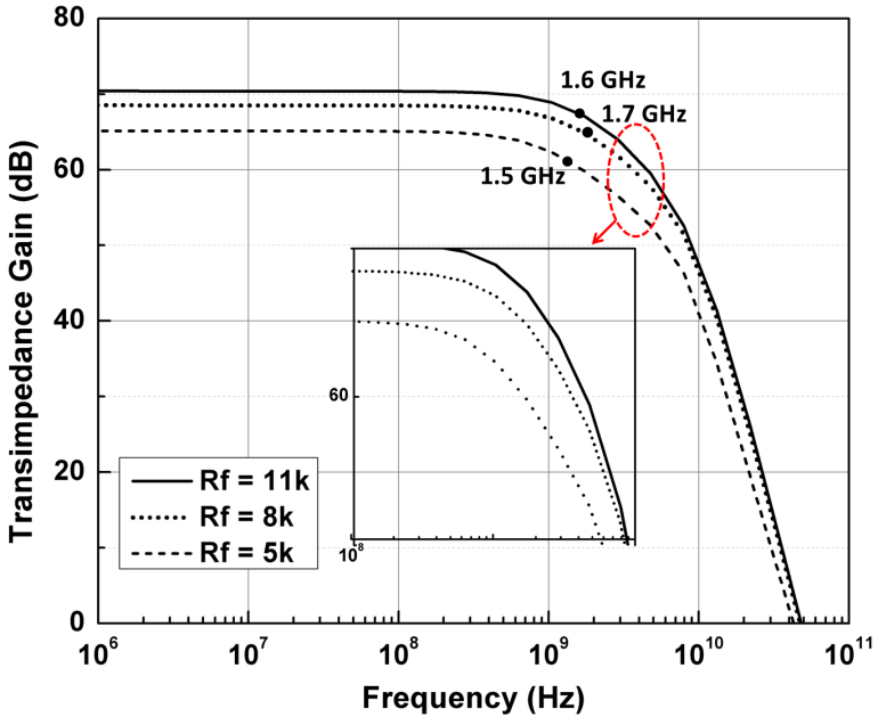


Fig. 5.9: Simulated frequency response of the proposed TIA with three different feedback resistor values (5, 8, and 11 kΩ) demonstrates non-constant gain-bandwidth product.

The cut-off frequency increases from 1.5 to 1.7 GHz as the feedback resistance rises from 5 to 8 kΩ. When the feedback resistance increases further from 8 to 11 kΩ, the bandwidth decreases from 1.7 to 1.6 GHz due to the reduction in the loop-gain at a high transimpedance gain. This can be improved by employing an output buffer to isolate the 50 Ω load from the feedback loop and is elaborated in detail in section V. Note that the gain-bandwidth products (GBP) are non-constant at different feedback resistance values, as shown in Table 5.2.

Table 5.2: Gain-bandwidth Product of the Proposed TIA

Proposed TIA	Rf = 5kΩ	Rf = 8kΩ	Rf = 11kΩ
GBP (dBΩGHz)	97.5	117.3	112

5.4 Noise

The principal noise sources in a SiGe HBT are shot noise and flicker noise in the base dc bias current I_B and shot noise in the collector dc bias current I_C [58]-[59]. Fig. 5.10 (a) shows the noise model of a common-emitter amplifier where I_{shb} and I_{fb} are the shot and flicker noise currents in the dc base current, and I_{shc} is the shot noise current in the dc collector current [58]-[59]. V_{th1} and V_{th2} are the thermal noise generated by R_1 and R_2, respectively. The external base and emitter circuits are replaced with the *Thevenin* equivalents in Fig. 5.10 (b). The *Thevenin* voltage seen looking out of the base (V_{tb}) and emitter (V_{te}) of the HBT can be obtained by inspection.

$$V_{tb} = V_{in} + V_{th1} + (I_{shb} + f_{fb})R_1 \tag{17}$$

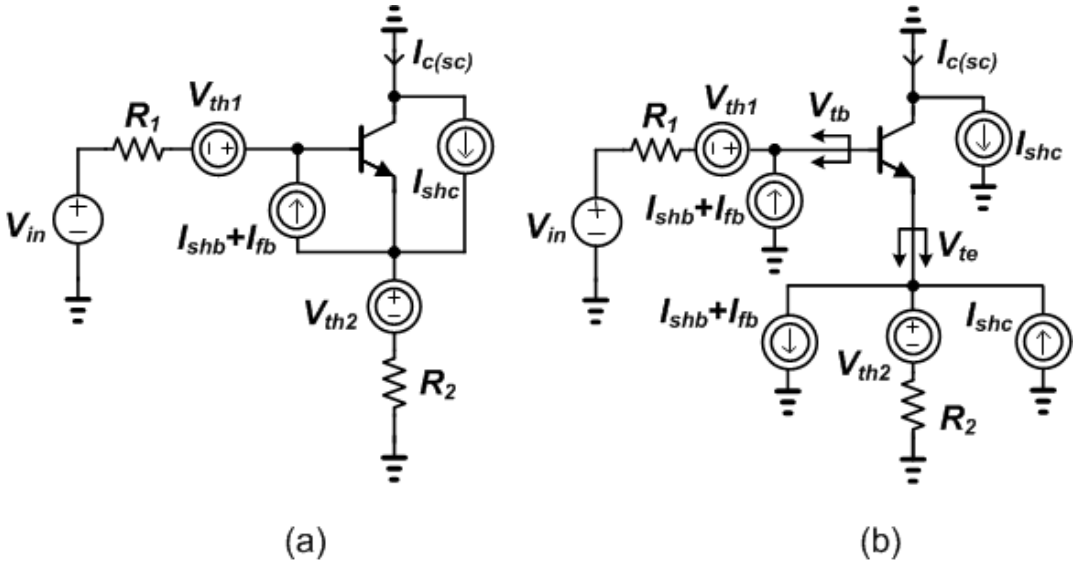


Fig. 5.10: (a) Common-emitter amplifier noise model. (b) Equivalent noise model to replace the external base and emitter circuits with the *Thevenin* equivalents.

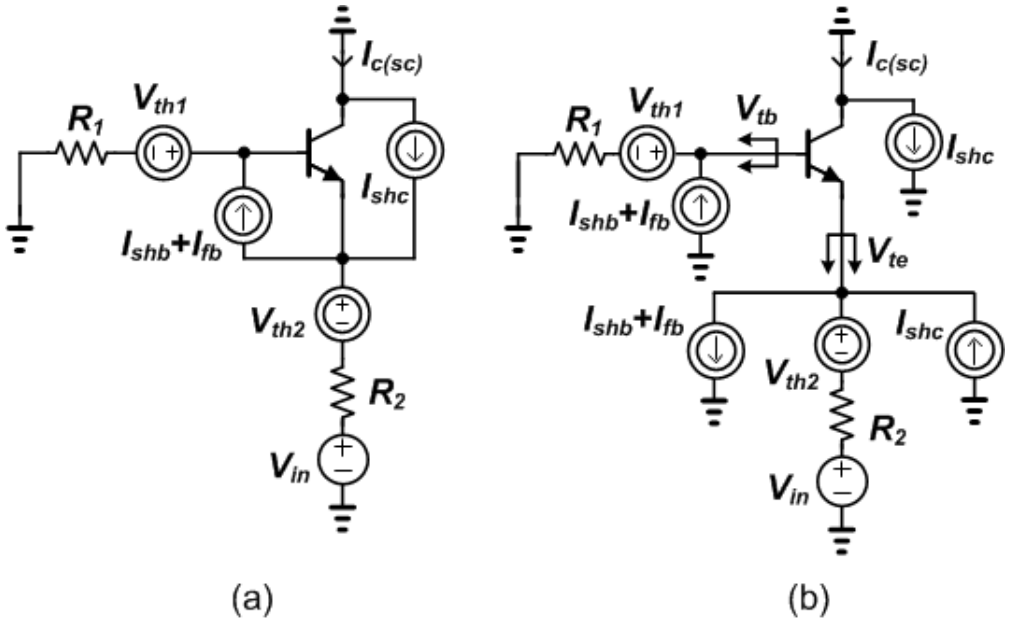


Fig. 5.11: (a) Common-base amplifier noise model. (b) Equivalent noise model to replace the external base and emitter circuits with the *Thevenin* equivalents.

$$V_{te} = V_{th2} + (I_{shc} - I_{shb} - I_{fb})R_2 \tag{18}$$

The *Norton* short-circuit current $I_{c(sc)}$ at the collector node in Fig. 5.10 (b) is derived to extract the input referred noise voltage V_{ni}, and it is given by

$$I_{c(sc)} = G_m(V_{tb} - V_{te}) = G_m\left[V_{in} + V_{th1} + (I_{shb} + I_{fb})R_1 - V_{th2} - (I_{shc} - I_{shb} - I_{fb})R_2 + \frac{I_{shc}}{G_m}\right] \tag{19}$$

where G_m is the overall transconductance. The input-referred noise voltage is given by

$$V_{ni} = \left[V_{th1} + (I_{shb} + I_{fb})R_1 - V_{th2} - (I_{shc} - I_{shb} - I_{fb})R_2 + \frac{I_{shc}}{G_m}\right] \tag{20}$$

The input-referred equivalent noise voltage V_{ni} is defined as the voltage in series with the source voltage V_{in} that generates the same noise voltage at the output as all noise sources in the circuit; in other words, it is the sum of all terms except V_{in} in (19). The mean-square values of shot and flicker noise currents are given by [58]

$$\bar{i_{sh}^2} = 2qI_{DC}\Delta f \tag{21}$$

$$\bar{i_f^2} = \frac{K_f I_{DC}^m \Delta f}{f^n} \tag{22}$$

where I_{DC} is the dc current, K is the flicker noise coefficient, m is the flicker noise exponent, and $n \approx 1$. By (17) - (22), the mean- square value of the input-referred noise can be written as

$$\bar{i_{sh}^2} = \left[\left(2qI_B \Delta f + \frac{K_f I_B \Delta f}{f} \right) (R_1 + R_2)^2 + 4KT(R_1 + R_2)\Delta f + 2qI_C \Delta f \left(\frac{R_1 + R_2}{\beta} + \frac{V_T}{I_C} \right)^2 \right] \quad (23)$$

where β is the common-emitter current gain and V_T is the thermal voltage.

The same procedure can be applied to the common-base amplifier in Fig. 5. 11 to show that the mean-square input-referred noise voltage of the common-base amplifier is identical to that of the common-emitter amplifier (23) if the dc bias condition and the values of R_1 and R_2 remain equal.

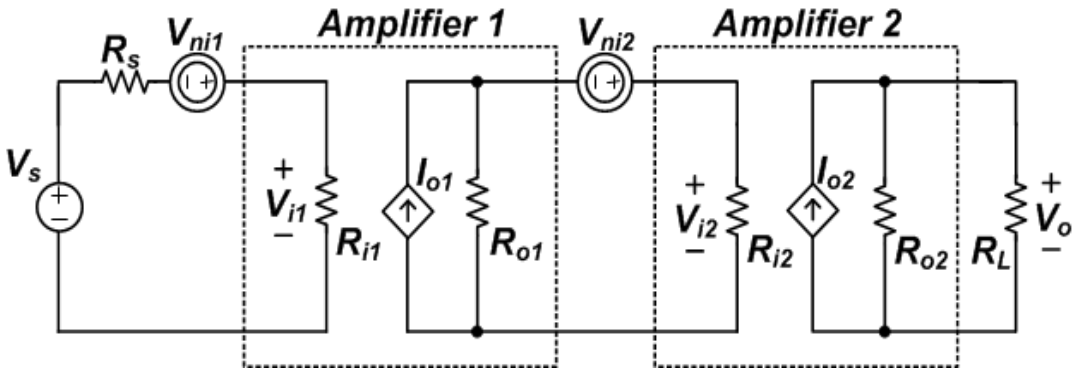


Fig. 5.12: Two stage amplifier noise model represents the proposed TIA. Amplifier 1 and 2 correspond to the common-base and the common-emitter stages of the proposed TIA, respectively.

Figure 5.12 shows the noise model of a two stage amplifier [58]. Amplifier 1 and Amplifier 2 stages in Fig. 5.12 correspond to the common-base and the common-emitter differential pairs of the proposed TIA, respectively.

By inspection, the output voltage V_o is given by ([58], [60])

$$V_o = A_v\left[V_s + V_{ni1} + \frac{V_{ni2}}{G_{m1}R_{o1}}\right] \tag{24}$$

where A_v is the total voltage gain through Amplifier 1 and 2 in shown in the figure. From (24), the input-referred noise V_{ni} for the proposed TIA can be obtained as

$$V_{ni} = V_{ni\_common\_base} + \frac{V_{ni\_common\_emitter}}{g_{m13}R_{c13}} \tag{25}$$

where g_{m13} is the transconductance of Q13 and R_{c13} is the equivalent impedance at the collector of Q13. Equation (25) illustrates that the equivalent input-referred noise of the proposed TIA is dominated by the sum of all internal noise in the common-base differential pair because the second term, the sum of all internal noise in the common-emitter differential pair, is divided by the gain of the common-base stage $g_{m13}R_{c13}$. Since the common-emitter and common-base amplifiers in Fig. 5.10 and 5.11 have the same input-referred noise (23) under the condition that the dc bias operating point and the values of R_1 and R_2 remain equal, the input-referred noise voltage of the proposed TIA is larger than that of the conventional TIA. The additional noise for the proposed TIA is equal to $V_{ni\_common\_emitter}/g_{m13}R_{b3}$. Furthermore, equations (23) and (25) imply that the input-referred noise of the proposed TIA can be noticeably reduced by decreasing the dc bias current of the common-base differential input stage while maintaining the dc bias of the common-emitter differential stage at the same level as that of the conventional TIA. PNP SiGe HBT devices were utilized in the common-base differential pair of the proposed TIA because at the same dc bias condition (I_C) the PNP SiGe HBTs exhibit higher transconductance and output impedance than NPN SiGe HBTs for the same size

for this technology. Hence, the additional input-referred noise in (25) for the proposed TIA can be further decreased.

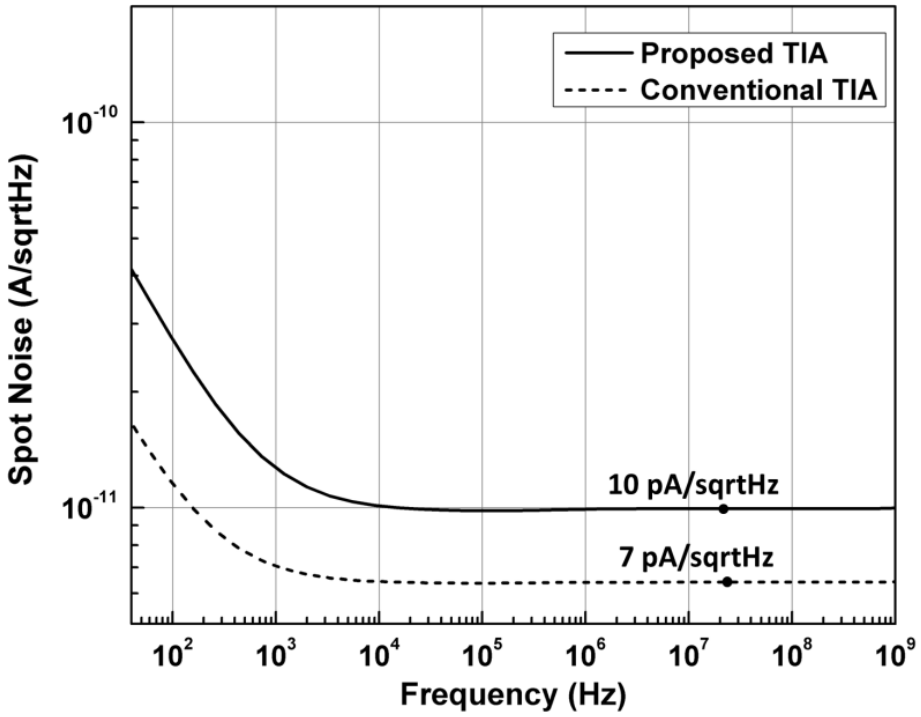


Fig. 5.13: Simulated input-referred spot noise of the conventional and proposed TIAs with the same gain of 8 kΩ. The noise values within the mid-band of the two TIAs are 7 and 10 pA/$\sqrt{Hz}$ for the conventional and proposed TIAs, respectively.

The simulated input-referred spot noise of the conventional and proposed TIAs with the same gain of 8 kΩ are shown in Fig. 5.13. The common-emitter differential stages of both the conventional and proposed TIAs are dc biased with 260 μA, and the common-base differential stage of the proposed TIA is biased with 350 μA. In the mid-band the spot noise of both the conventional and proposed TIAs are 7 and 10 pA/$\sqrt{Hz}$, respectively. The spot noise of the proposed TIA is higher than that of the conventional

TIA mainly because the dc bias current of the common-base differential stage is 26% higher than that of the common-emitter differential stage.

5.5 Output Buffer

To sufficiently drive a 50 Ω load, an output buffer is required. When the output of the proposed TIA (Fig. 5.3) is directly connected to the 50 Ω load, the increment of the bandwidth and transimpedance gain are limited especially at a high gain because the feedback network is affected by the 50 Ω load resistors, resulting in the decrease of the loop-gain. Thus, the TIA must be isolated from the load with an output buffer to achieve the gain-bandwidth improvement.

Another requirement for an output buffer is the capability of supplying a large current to the 50 Ω load. Thus, the input transistors of the buffer need to be relatively large in size compared to the ones in the TIA. This can cause a degradation in the bandwidth due to the large base-emitter parasitic capacitances of the input devices. To minimize the effect of these parasitic capacitances an f_T-doubler output buffer, shown in Fig. 5.14, is utilized [61]. The effective input capacitance seen looking into the base of Q25 of the output buffer is approximately reduced by a factor of 2.

$$C_{be25\_effective} = \left(\frac{1}{C_{be25}} + \frac{1}{C_{b26}} \right)^{-1} = \frac{C_{be25}}{2} \tag{26}$$

The simulated frequency response of the proposed TIA with the f_T-doubler output buffer is shown in Fig. 5.15. Cascaded with the output buffer, the cut-off frequencies with 5 and 8 kΩ feedback resistors increase from 1.5 to 1.9 GHz and 1.7 to 2.7 GHz, respectively.

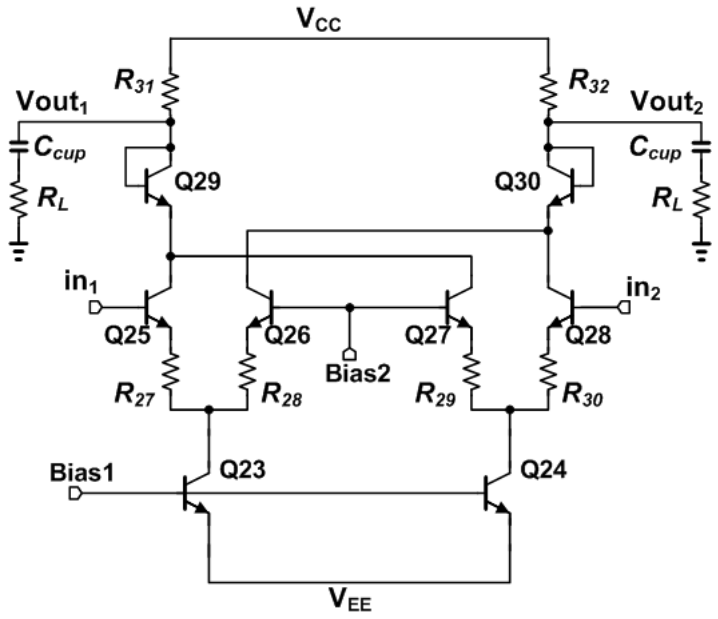


Fig. 5.14: The f_T -doubler output buffer isolates the TIA from the 50 Ω load and supplies a large current to the 50 Ω load.

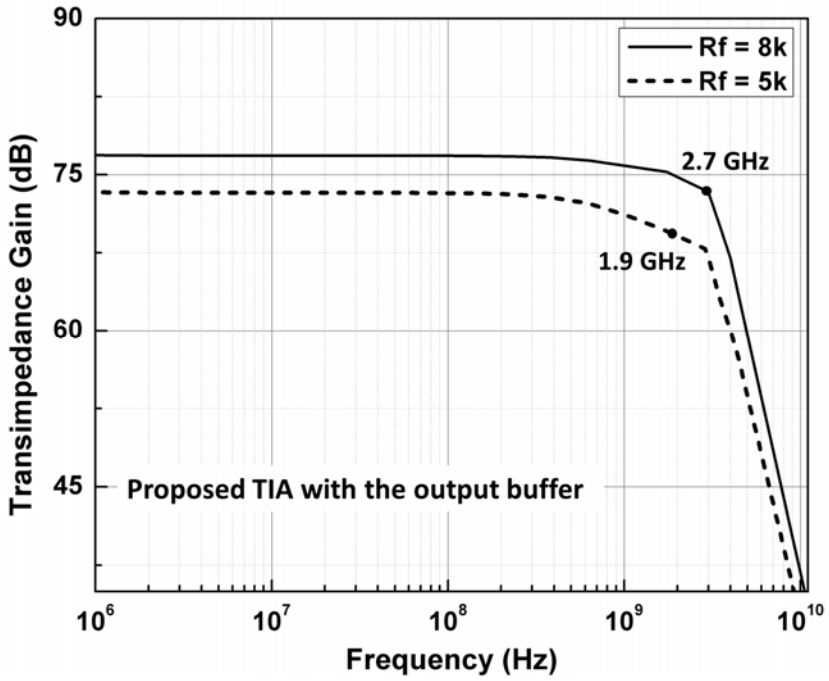


Fig. 5.15: Simulated frequency response of the proposed TIA with the f_T - doubler output buffer. The cut-off frequencies with 5 and 8 kΩ feedback resistors increase from 1.5 to 1.9 GHz and 1.7 to 2.7 GHz, respectively, with the output buffer.

The gain-bandwidth products at 5 and 8 kΩ feedback resistors with the output buffer are 140.6 and 210.6 dBΩGHz, demonstrating a non-constant gain-bandwidth product, as claimed.

5.6 Measurements

Three circuits were fabricated utilizing a complementary SiGe HBT on SOI technology ([8], [15], [56]) as shown in Fig. 5.16: (a) the proposed TIA with R_f = 5 kΩ, (b) the proposed TIA with R_f = 8 kΩ, and (c) the conventional TIA with R_f = 8 kΩ. The proposed TIAs with 5 kΩ (a) and 8 kΩ (b) feedback resistors are to verify the concept of designing a TIA with non-constant gain-bandwidth product. Their layouts are identical except for the feedback resistor values. The proposed TIA (b) and the conventional TIA (c) enable a comparison of the noise performance (spot noise) at the same transimpedance gain of 8 kΩ.

The frequency responses of the two proposed TIAs with 5 and 8 kΩ feedback resistors were measured using an Agilent E8361C PNA Network Analyzer and plotted in Fig. 5.17. As illustrated in the plot, when the transimpedance gain increases (from 5 to 8 kΩ) the bandwidth increases from 1.4 to 2.2 GHz demonstrating the non-constant gain-bandwidth product. The measurement results closely correspond to the simulation results, as can be seen in Fig. 5.15.

The spot noises of the conventional and proposed TIAs with the same gain of 8 kΩ, between 200 MHz and 500 MHz, were measured using an Agilent E4446A Spectrum Analyzer. Fig. 18 shows that the average spot noise of the proposed TIA is 25% higher than that of the conventional TIA at the same gain. The average spot noises for the conventional and proposed TIAs are 30 and 40 pA/$\sqrt{Hz}$, respectively. The spot noise of

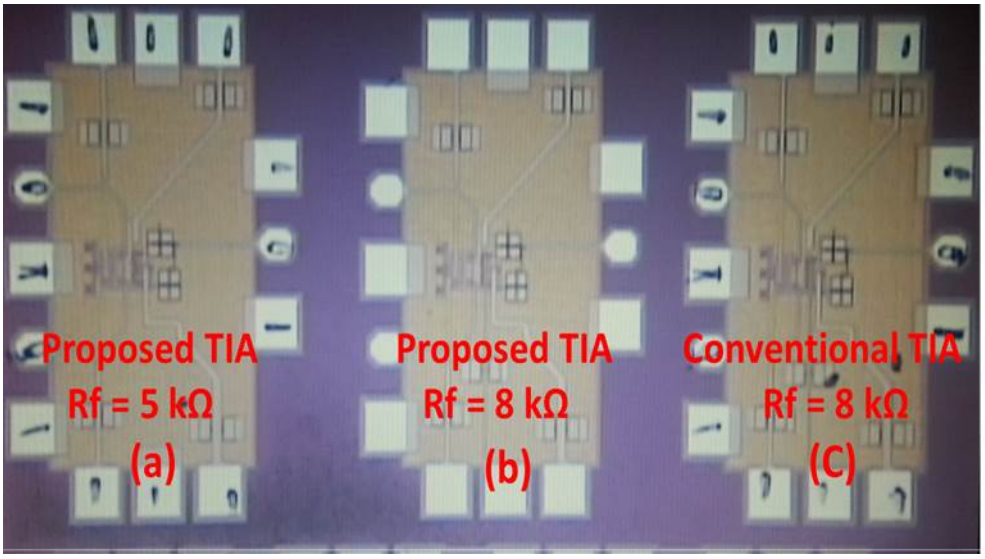


Fig. 5.16: Three fabricated circuits utilizing a complementary SiGe HBT on SOI technology to verify non-constant gain-bandwidth product (a and b) and to compare noise performance (b and c).

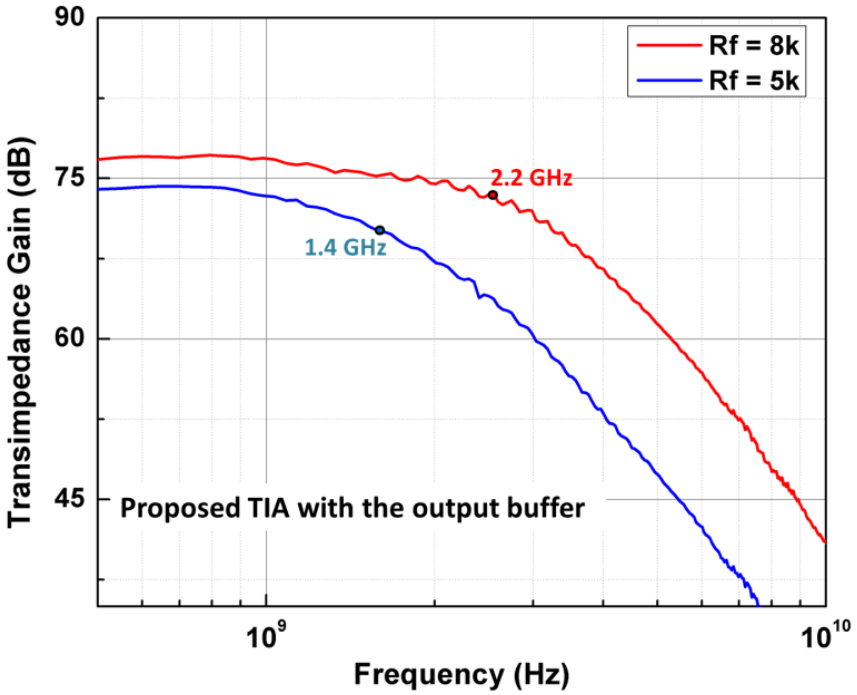


Fig. 5.17: Measured frequency response of the proposed TIA with the f_T - doubler output buffer.

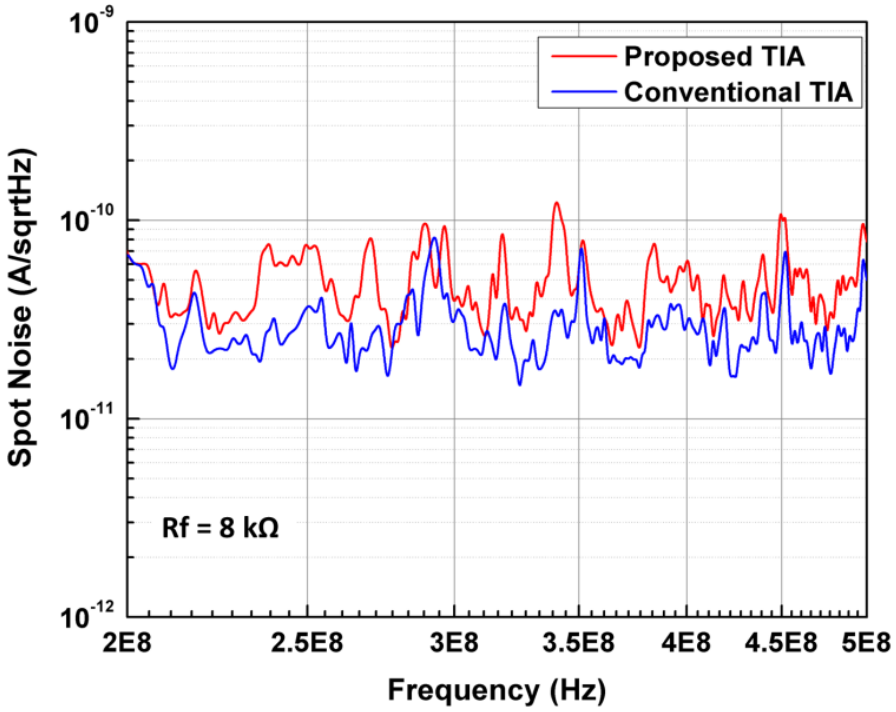


Fig. 5.18: Measured input-referred spot noise of the conventional and proposed TIAs in A/$\sqrt{Hz}$. The average noise values are 30 and 40 pA/$\sqrt{Hz}$ for the conventional and proposed TIAs, respectively; they are measured between 200 and 500 MHz.

the proposed TIA is higher than that of the conventional TIA mainly because the dc bias current of the common-base differential stage of the proposed TIA is higher than that of common-base differential stage of the conventional TIA.

Table 5.3 summarizes the performance of the conventional and the proposed TIAs. The bandwidth of the proposed TIA is 7 times larger than that of the conventional TIA at the same gain of 78 dBΩ. The input-referred spot noise and the dc power consumption of the proposed TIA are higher by 25% and 18%, respectively, than those of the conventional TIA. Note that the bandwidth of the proposed TIA increases 36% as the transimpedance gain rises from 74 dBΩ to 78 dBΩ, as shown in Table 5.3. Consequently, the product of the gain and bandwidth rises from 103.6 to 171.6 dBGHz, demonstrating the efficacy of using a design exploiting a non-constant gain-bandwidth product.

Table 5.3: Performance Comparison between Conventional and Proposed TIAs

TIA	Gain (dBΩ)	BW (GHz)	GBP (dBGHz)	Spot Noise^{+} (pA/sqrtHz)	Power (mW)
Conventional with 8 kΩ	78	0.3	23.4	30	23
Proposed with 8 kΩ	78	2.2	171.6	40	28
Proposed with 5 kΩ	74	1.4	103.6	47	28

5.7 Summary

Two techniques to increase the gain and bandwidth in transimpedance amplifiers were demonstrated in this work. The input impedance was reduced and a non-constant gain-bandwidth product was achieved using global feedback with a common-base differential input stage. Three TIAs with a 2 pF parasitic input photo-diode capacitance were fabricated and measured on a complementary SiGe HBT on SOI platform with a peak f_T of 50 GHz. The bandwidth of the proposed TIA is more than 7 times higher than that of the conventional TIA for the same transimpedance gain (8 kΩ). The bandwidth of the proposed TIA increased as the transimpedance gain rose from 5 to 8 kΩ, demonstrating the non-constant gain-bandwidth products of 103.6 and 171.6 dBΩGHz, respectively. However, these gain-bandwidth improvements come at the cost of a slightly higher input-referred spot noise; the proposed TIA has 25% higher spot noise than that of the conventional TIA for the same gain.

5.8 Acknowledgement

Seungwoo Jung is thankful to Texas Instruments SiGe team for their support.

CHAPTER 6

THE ROLE OF NEGATIVE FEEDBACK EFFECTS ON SINGLE-EVENT TRANSIENTS IN SIGE HBT ANALOG CIRCUITS

6.1 Introduction

Negative feedback reduces noise and distortion in a circuit and increases signal-to-noise ratio (SNR) [57], [62], [63]. It decreases the sensitivity of a circuit to parameter variations and other undesirable changes due to the ambient environment and manufacturing tolerances. Technically speaking, a single event transient caused by a heavy ion striking a sensitive node in a microelectronic system can be thought of as a noise source, because the resulting transient response in the output signal does not require an input signal to be generated. Thus, feedback theory implies that negative feedback can lessen the impact of a single event transient (SET) in an electronic system, thereby helping its rapid recovery.

In order to investigate the role of negative feedback effects on single-event transients in circuits, two different types of current mirrors (a basic common-emitter current mirror and a Wilson current mirror) were fabricated using a silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) BiCMOS technology, and exposed to laser-induced single events.

SiGe HBTs have received extensive attention for implementation in extreme environment applications due to their excellent total-ionizing-dose (TID) radiation tolerance, high-speed operation (i.e., high unity gain frequency f_T), superb cryogenic performance, and ease of integration within a complementary metal-oxide semiconductor (CMOS) platform [23]. However, studies have shown that SiGe HBTs are susceptible to single event phenomena [31]. Thus, it is highly desirable that single-event performance of

SiGe HBT circuits be improved, either via device or circuit design, or both. In order to reduce the sensitivity of SiGe HBTs to single event transients, various hardening methodologies, both at the device and design level, have been developed [33]. For example, it has been demonstrated that SiGe HBTs in inverse-mode have an improved SEU response [42].

This work demonstrates in detail how adding internal or external negative feedback can reduce the impact of single event transients. We use signal flow graph theory to better understand and illustrate this [5]. To examine the effects of both internal and external feedback, basic common-emitter NPN current mirrors, with and without internal feedback, Wilson current mirrors, and Wilson mirrors with intrinsic external feedback removed, are examined under the influence of laser-induced single event transients. All experimented current mirrors were fabricated utilizing IBM 8HP 130 nm SiGe BiCMOS technology.

6.2 Negative Feedback

Noise and distortion can be generated anywhere in a circuit. Noise is an undesired signal at the output of a circuit when the input signal is absent. Most common types of noise are thermal noise (Johnson noise), low-frequency noise (flicker or 1/f noise), shot noise, and burst noise (popcorn or G/R noise). On the contrary, distortion is an undesired signal at the output of a circuit with an input signal present. Common types of linear distortion are gain error and phase shift, and common types of non-linear distortion include peak clipping, current limiting, and slew rate limiting. One of the desired features of negative feedback is that it reduces both noise and distortion if the feedback loop-gain is greater than unity [58].

Fig. 6.1 illustrates an amplifier model with noise and distortion added. The gain stage is divided into two sub-gain stages (A_1 and A_2) in order to model noise and distortion generated inside and outside the circuit by adding an external source v_{ND}

between the two gain stages (note that v_{ND} includes both noise and distortion). The output voltage can be expressed as

$$v_{OUT} = \frac{A_1 A_2}{1 + A_1 A_2 \beta} v_{IN} + \frac{A_2}{1 + A_1 A_2 \beta} v_{ND} \tag{1}$$

where β is the feedback factor. Both the noise and distortion are reduced by the amount of feedback ($1+A_1A_2\beta$) of the amplifier, as depicted in equation (1). Three important observations can be made from this equation. First, if the noise and distortion are present at the input of the amplifier, the reduction of them by negative feedback is insignificant; the noise and distortion are reduced only by β instead of ($1+A_1A_2\beta$), assuming $A_1A_2\beta$ is much greater than unity. Second, the higher the amount of feedback is increased, the lower the effects of the noise and distortion become in the output signal of the amplifier. From (1), the ratio of the signal to the noise as well as distortion in the output signal ($Ratio_{SND}$) can be calculated as

$$Ratio_{SND} = \frac{\left(\frac{A_1 A_2}{1 + \beta A_1 A_2}\right) v_{IN}}{\left(\frac{A_2}{1 + \beta A_1 A_2}\right) v_{ND}} = A_1 \frac{v_{IN}}{v_{ND}} \tag{2}$$

As shown in equation (2), this ratio is independent of the amount of feedback present. However, the signal-to-noise/distortion ratio can be improved with negative feedback if the input voltage is increased so that the output signal remains constant; in this case, the output signal component caused by the noise and distortion becomes smaller than the output signal component caused by the input signal in (1) as the input increases. For instance, if the gain of an amplifier is reduced to 10% of its original value by adding

feedback, and, at the same time, the input is increased to regain the same original output voltage, the percent noise and distortion in the output signal with respect to the input signal reduces to 10% of its original value. Thus, a useful observation can be made from equation (1): in order to improve signal-to-noise/distortion ratio by adding negative feedback, the output signal must be maintained constant by increasing the input signal level simultaneously.

A single event transient is a noise (not distortion) to a system because an input signal is not required for the generation of the corresponding noise output. Therefore, all the theoretical observations made above on negative feedback can in principle be utilized to reduce the single event transients in a system.

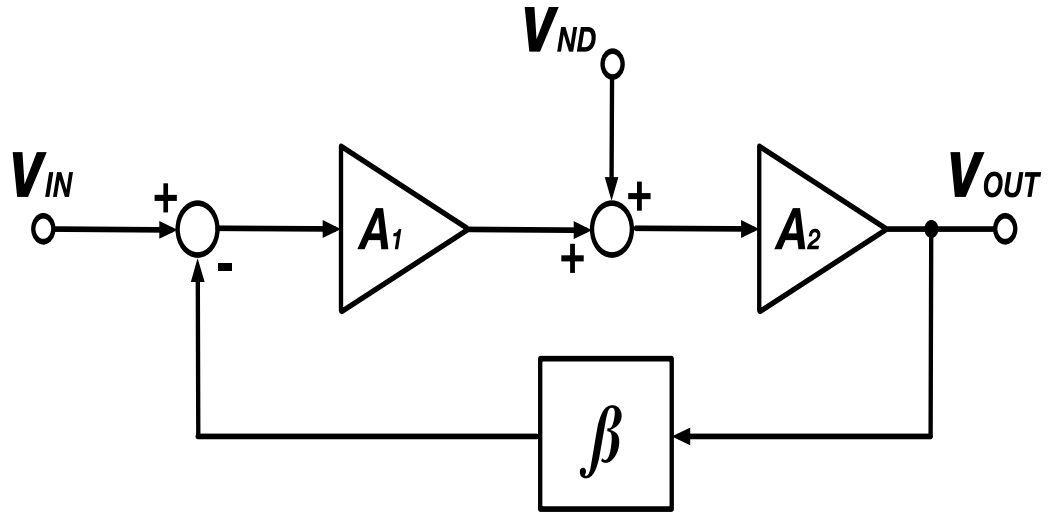


Fig. 6.1: Amplifier model with noise and distortion added as an external source v_{ND}. Here, v_{ND} includes both noise and distortion.

6.3 Current Mirrors with Negative Feedback

Two current mirror topologies are explored here in order to study the effects of negative feedback in circuits with respect to single event transients: a basic common-emitter current mirror, with and without internal feedback, and a Wilson current mirror, with and without external feedback. Current mirrors are one of the most essential and fundamental DC bias blocks in integrated circuits, and virtually all analog and RF circuits utilize current mirrors to establish their DC bias. Experiments and analysis of single event transients in current mirrors can be accurately performed, and the results of the analysis can be readily applied to predict feedback effects in other complex circuits because they are DC circuits (i.e., no AC input signal is required), and their structures are simple to implement.

The negative feedback loops in the current mirrors are broken instantaneously at the occurrence of a single event because the DC bias conditions of the circuits are disturbed by the high-speed (pulse width = 175 fs) and large signal (as opposed to small signal) TPA laser. As a single event transient dies out after breaking the DC bias condition, the circuits will try to recover their original quiescent state, and the negative feedback helps recovery because it increases the bandwidth of a circuit.

The basic common-emitter current mirrors tested and analyzed are shown in Fig. 6.2. Adding an emitter resistor RE in a common-emitter configuration, as shown in Fig. 6.2 (b), creates an internal negative feedback. The feedback is called internal because its loop is invisible. A small value of RE is often added to match the output current more closely to the reference current and to avoid the thermal runaway in the collector current of HBTs; the resistance value must remain small not to turn a transistor off by reducing the base-emitter voltage (V_{BE}). Adding an emitter degeneration resistor (RE) at the emitter of the output device (Q2) will decrease the output current unless the same value of resistor is added at the emitter of the reference device (Q1).

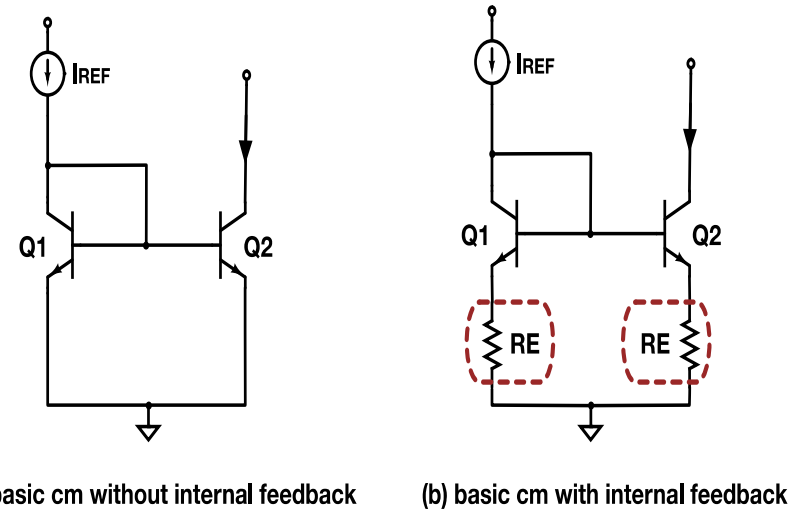


Fig. 6.2: Basic common-emitter current mirror (cm) with (a) and without (b) internal negative feedback.

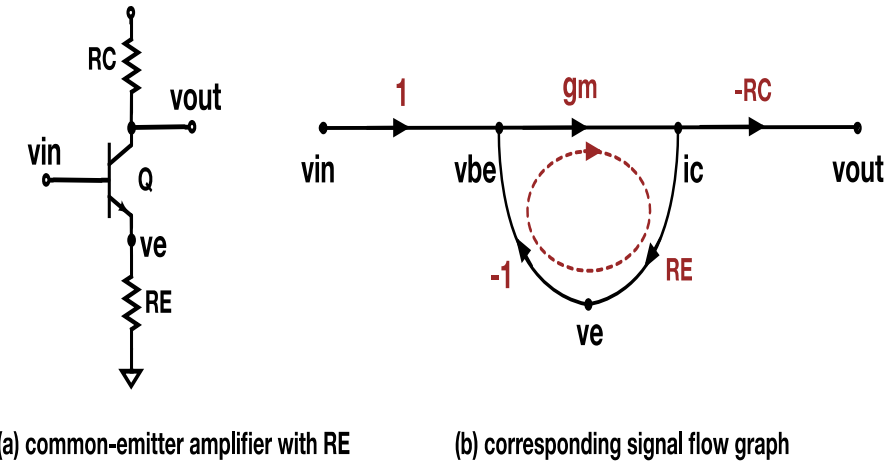


Fig. 6.3: Common-emitter amplifier with emitter degeneration resistor RE (a), and its corresponding signal flow graph (b).

In order to make the feedback loop visible and analysis simple, signal flow graph theory is employed in Fig. 6.3 (b). The internal feedback loop (dotted red line) is clearly visible in the signal flow graph, and its polarity is negative because there is one inversion between the v_e and v_{be} nodes around the loop; an odd number of inversions creates negative polarity. The feedback network allows the input and output to communicate with each other, so as to reduce the sensitivity to unexpected changes by the amount of feedback in the circuit. For example, the collector current of a SiGe HBT increases as the temperature increases, and if not controlled, this thermal runaway can cause a malfunction. However, the internal feedback via the emitter degeneration prevents thermal runaway by the following mechanism. As the collector current rises (runaway), the emitter voltage (v_e) rises as well due to the emitter resistor RE, which in turn decreases the base-emitter voltage (v_{be}), leading to a decrease in the collector current; hence negative feedback.

The amount of feedback (Δ_{CE}) in the basic common-emitter current mirror with emitter degeneration resistor RE can be gained by inspection of the signal flow graph in Fig. 6.3 (b), and is expressed in equation (3) where g_m is the transconductance of the HBT.

$$\Delta_{CE} = 1 - g_m \times RE \times (-1) = 1 + g_m RE \tag{3}$$

Since the noise and distortion in a system are reduced by the amount of feedback, as discussed previously, a single event transient can be reduced by increasing the transconductance (g_m) and RE in (3). Transconductance g_m is given as

$$g_m = \frac{I_C}{V_T} = \frac{I_C}{\frac{KT}{q}} \tag{4}$$

where I_C, K, T, and q are the DC collector current, Boltzmann's constant, the Kelvin temperature, and electronic charge respectively. Thus g_m can be set at a desired value by varying the DC collector current I_C, which can be set by the reference current I_{REF}. The reference current (I_{REF}), in many applications, is created by a bandgap circuit with an op-amp so that it remains independent of temperature variation.

Wilson current mirrors contain an external negative feedback loop (red dotted line), as shown in Fig. 6.4 (a); the feedback is called external here because its loop is clearly visible in the circuit. In order to investigate external feedback effects in single event transients, the feedback loop is removed from the Wilson mirror, as shown in Fig. 6.4 (b). The loop is broken at the highest impedance node between the collector of Q1 and the base of Q3 to mitigate loading effects. The feedback network in the Wilson current mirror is replaced with *Thevenin* equivalents in Fig. 6.5 (a) to simplify the AC analysis. The corresponding signal flow graph is constructed in Fig. 6.5 (b), assuming $\alpha_1 = 1$ (i.e. $i_{e1} = i_{c1}$). The amount of feedback (Δ_W) can be determined by inspection of the flow graph, and it is expressed in equation (4) where G_{m1} and G_{m3} are the overall (or effective) transconductance of device Q1 and Q3, respectively, g_{m2} is the transconductance of Q2, and

$$\Delta_W = 1 - G_{m1} \times (-r_{ic1}) \times G_{m3} \times \frac{1}{g_{m2}} = 1 + \frac{G_{m1} G_{m3} r_{ic1}}{g_{m2}} \tag{4}$$

r_{ic1} is *Thevenin* equivalent resistance seen looking into the collector of Q1. The gain through the feed-forward path is ignored in the Δ_W calculation because its value is minimal. The amount of feedback of the Wilson mirror can be increased by decreasing g_{m2} and increasing G_{m1}, G_{m3}, and r_{ic1} according to (4), in order to improve noise performance.

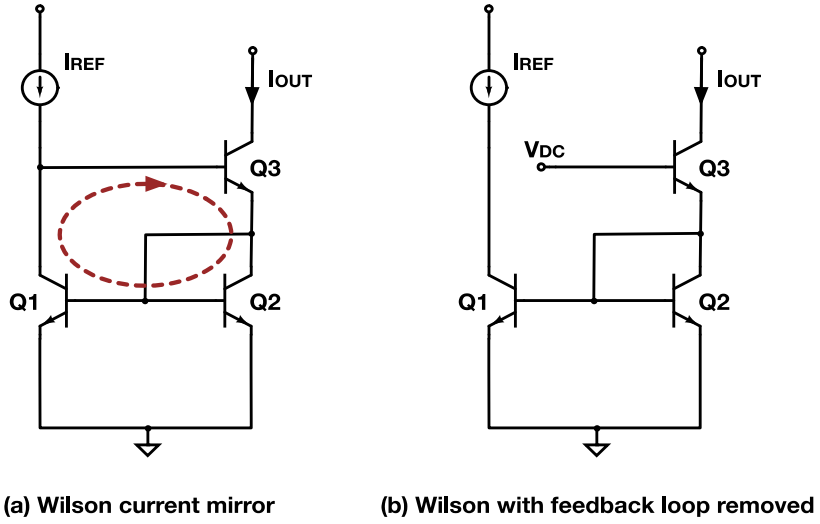


Fig. 6.4: Wilson current mirror (a) and Wilson mirror with external feedback loop removed (b). The feedback loop is broken at the highest impedance node between the collector of Q1 and the base of Q3 to minimize loading effects.

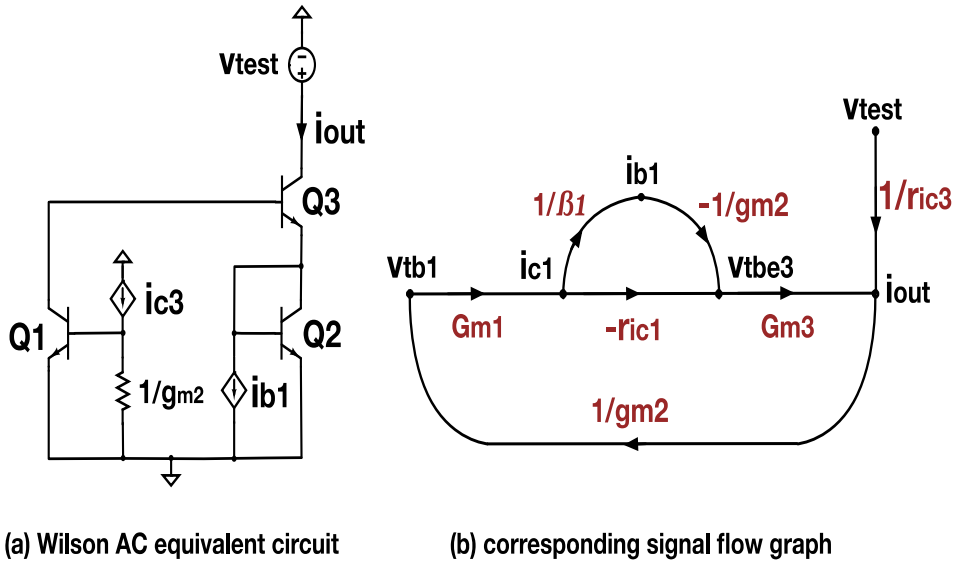


Fig. 6.5: Wilson AC equivalent circuit with feedback loop replaced (not removed) with Thevenin equivalent circuits (a) and corresponding signal flow graph (b).

The output resistance of the standard common-emitter current mirror is given by

$$r_{out\_CE} = r_{ic2} = r_{o2} = \frac{V_{A2} + V_{CE2}}{I_{C2}} \tag{5}$$

where V_{A2} is the Early voltage of Q2. A test voltage (v_{test}) is added at the output of the Wilson mirror to calculate its output resistance. The output resistance from the signal flow graph is given by

$$r_{out\_Wilson} = \left(\frac{i_{out}}{v_{test}} \right)^{-1} = \left(\frac{1}{\Delta_W} \times \frac{1}{r_{ic3}} \right)^{-1} = \Delta_W r_{ic3} \tag{6}$$

where r_{ic3} is the *Thevenin* equivalent resistance seen looking into the collector of Q3, which is given by

$$r_{ic3} = \frac{r_{o3} + r_{ie3} \,||\, R_{te3}}{1 - \alpha_3 \dfrac{R_{te3}}{r_{ie3} + R_{te3}}} \tag{7}$$

R_{te3} and r_{ie3} are the *Thevenin* equivalent resistance seen looking out of and looking into the emitter of Q3, respectively. Here, α_3 is the common-base current gain, which is close to unity.

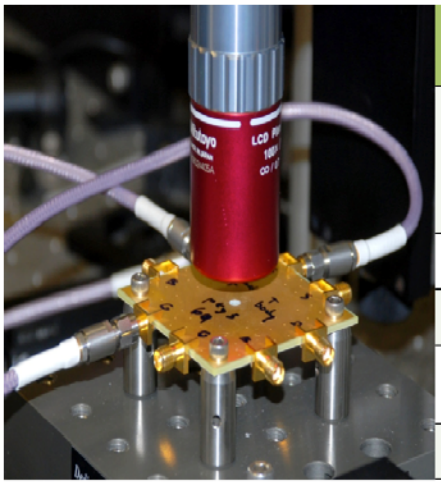
As shown in equation (5) - (7), one of the main differences between the standard common-emitter and the Wilson current mirror is their output resistance. If all transistors used in the current mirrors have the same physical dimensions (true for this study), and their DC bias current is the same (I_{REF} = 500 μA), then $r_{o2} = r_{o3} = r_{o,}$ assuming their Early voltage (V_A) is much greater than their collector-emitter voltage (V_{CE}). For that case,

while the output resistance of the standard common-emitter current mirror is the same as the intrinsic output resistance of Q2 (r_o), the output resistance of the Wilson mirror is increased to be much greater than that of the common-emitter mirror by the two feedback elements, as described in (6) and (7); the intrinsic external feedback as well as the internal feedback caused by the resistance seen looking out of the emitter of Q3. As a result, the output of the Wilson mirror is closer to the ideal current source, whose output resistance is infinity, than that of the standard common-emitter current mirror. However, the main drawback of Wilson mirror is that it requires a higher supply voltage than the common-emitter current mirror.

Note that increasing an amount of feedback decreases the overall gain of a circuit such as an operational amplifier. Thus there will be a rather strict limitation in the maximum value of an amount of feedback for the applications that require very high gain. If both a reliable SE performance and high gain are required at the same time, cascading multiple low-gain feedback amplifiers might be a solution.

6.4 Experimental Setup

Single-event transient (SET) measurements were performed at the U.S. Naval Research Laboratory (NRL) using a two-photon absorption (TPA) pulsed laser single event effect (PLSEE) through wafer technique [62]. The TPA PLSEE system at NRL is depicted in Fig. 6.6, together with its specifications. The samples under test were packaged using a high-speed custom-designed printed circuit board, Southwest Microwave SMA end launchers, low loss SMA cables, Keithley 2400 DC power supplies, and RF bias tee's. Single event transients (SETs) were measured through a Tektronix high-speed DPO71254 12.5 GHz real time oscilloscope. The energy level of the TPA pulsed laser was set to 3158 pJ throughout the experiment.



Naval Research Laboratory	
Equipment	Clark-MXR CPA1000 Amplified Titanium Sapphire Laser System
Pulse Width	150 fs
Wavelength	1260 nm (0.98 eV)
Laser Repetition Rate	1 kHz
Focal Spot Size	1 μm

Fig. 6.6: Two-photon absorption (TPA) pulsed laser system and its main specifications at the Naval Research Laboratory (NRL).

6.5 Internal Negative Feedback

2-D TPA pulsed laser raster scans were performed on the basic common-emitter current mirrors, both with and without the internal negative feedback, under the DC bias condition of I_{REF} = 500 μA. The resulting 2-D raster scan plots showing the peak output transient current are found in Fig. 6.7. The most noticeable difference that can be observed from the two plots is that the internal negative feedback created by simply adding the emitter degeneration resistor RE at the emitters of the basic current mirror reduces the highest peak output transient current by one-half (from 2 mA to 1 mA), clearly a significant reduction.

The charge induced by single event transients increases the output current (collector current of Q2), which leads to an increased voltage drop across the emitter resistors (REs). The additional voltage drop across the resistor will trigger a feedback mechanism, where the base-emitter voltage v_{BE} (or error voltage) will decrease for a fixed base voltage, leading to a decrease in the output current to the original value prior to the single-event transient, because the collector current of a SiGe HBT is exponentially

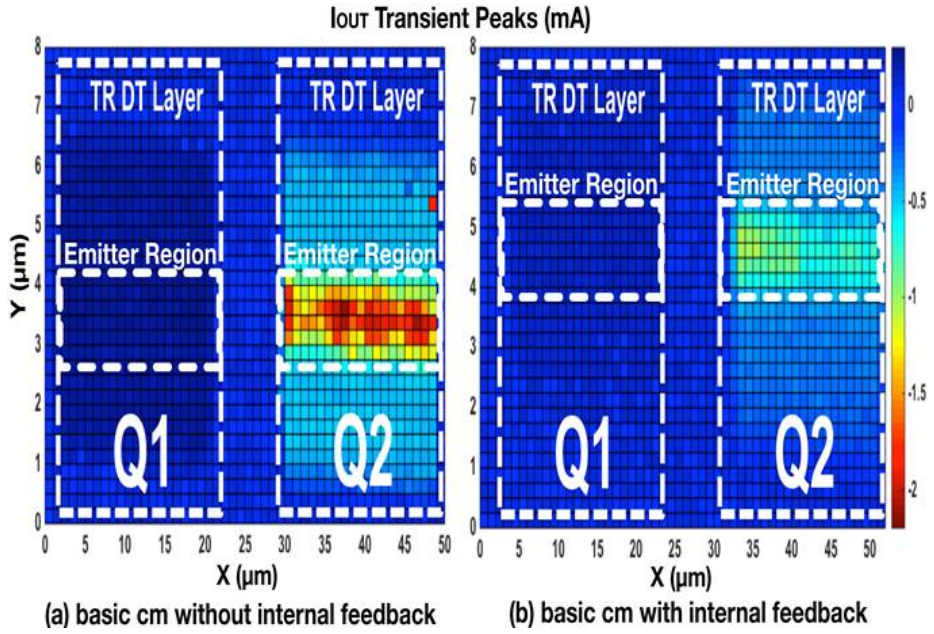


Fig. 6.7: 2-D raster scan plots show the peak output transient current as Q1 and Q2 of the basic common-emitter current mirrors are impacted by the TPA laser. The highest peak output transient current in the mirror with internal feedback is 50% lower than that of the mirror without feedback.

proportional to the base-emitter voltage v_{BE}, as shown in (8), where I_S is the saturation current, and V_T is the thermal voltage.

$$i_C = I_S e^{\frac{v_{BE}}{V_T}} \tag{8}$$

The transient in the output current is smaller when the input device Q1 is struck by the laser than when the output device Q2 is struck, because the input device Q1 is diode-connected, which is in itself a form of local negative feedback [3]. The output transient current of the basic common-emitter current mirror, both with and without internal negative feedback, is plotted in the time domain (Fig. 6.8) as a fixed physical

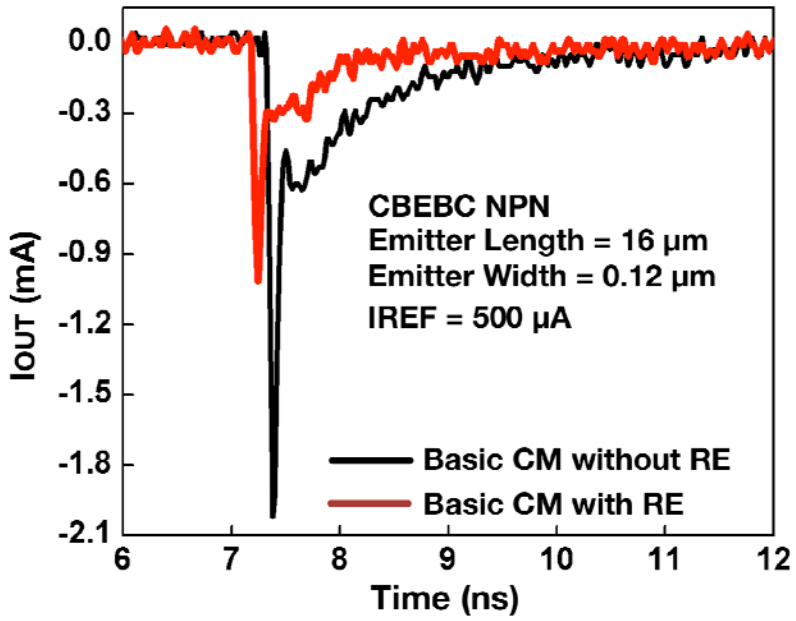


Fig. 6.8: The internal negative feedback in the common-emitter current mirror reduces the peak output transient current and recovery time as the output device Q2 is impacted by the TPA laser.

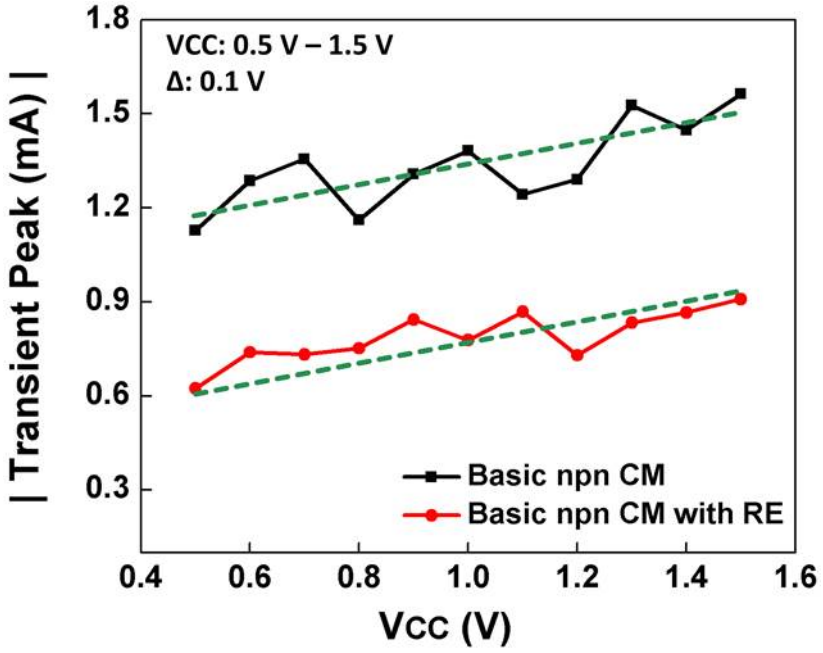


Fig. 6.9: The supply voltage (V_{CC}) of the common-emitter NPN mirrors is swept from 0.5 V to 1.5 V with a step of 0.1 V during the laser strike to investigate supply dependence of SET response.

location on Q2 is struck by the laser. The peak transient of the mirror with internal feedback is significantly smaller than that of one without feedback. The settling time of the mirror with internal feedback is also shorter (i.e., faster recovery from a SET) than that of the one without internal feedback.

The supply voltage (V_{CC}) was swept from 0.5 V to 1.5 V in 0.1 V steps during the laser exposure (Fig. 6.9) in order to study the supply voltage influence upon the SET response. With the base-emitter voltage v_{BE} determined by the reference current value (I_{REF}), the collector-base potential increases as the supply voltage rises, which leads to an increased avalanche generation within the device. This increase in avalanche generation produces additional electron-hole pairs which add to those created by the laser strike, thereby increasing the peak transient current as the supply voltage increases (Fig. 6.9). The figure highlights the diminished peak transient with the internal negative feedback consistently while the supply voltage (VCC) was swept.

6.6 External Negative Feedback

2-D TPA pulsed laser raster scans were conducted on the Wilson current mirror and the Wilson mirror with its intrinsic external feedback removed, under the DC bias condition of I_{REF} = 500 μA. The resulting 2-D raster scan plots showing the peak output transient current are drawn in Fig. 6.10 as the two bottom transistors (Q1 and Q2) are laser scanned. The output device Q3 is separately scanned. The reduction in the highest peak output transient current is 62% (from 3.7 mA to 1.4 mA) in the Wilson current mirror compared to the Wilson mirror with the external feedback removed, when Q1 is struck by the laser. However, as with the basic common-emitter current mirrors, the difference between the highest transient peaks in the output current of the two current mirrors is subtle when Q2 is struck, due to the local negative feedback provided by the diode-connection [42].

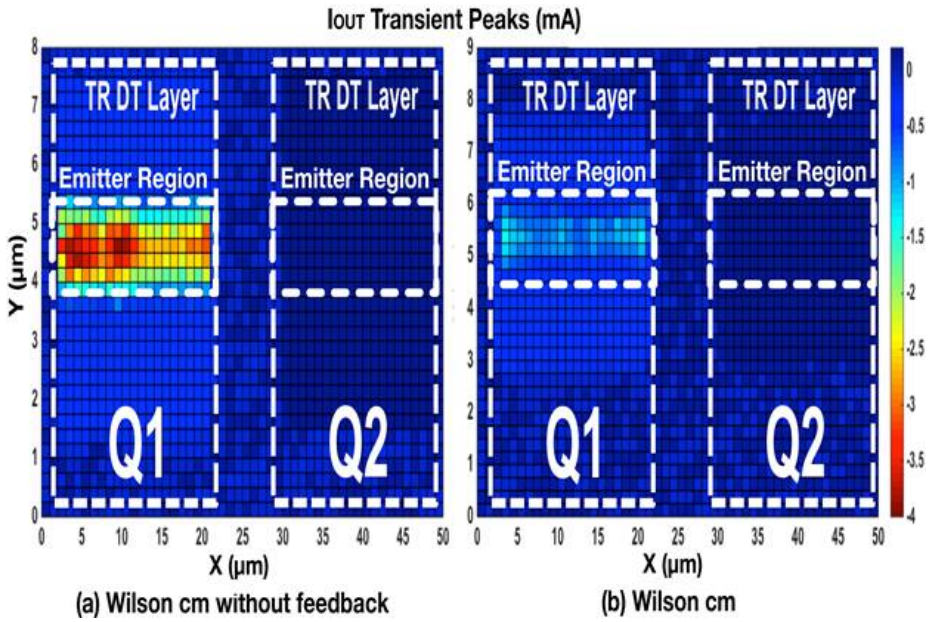


Fig. 6.10: 2-D raster scan plots show the peak output transient current as Q1 and Q2 of Wilson current mirror with (a) and without (b) external feedback are impacted by TPA laser.

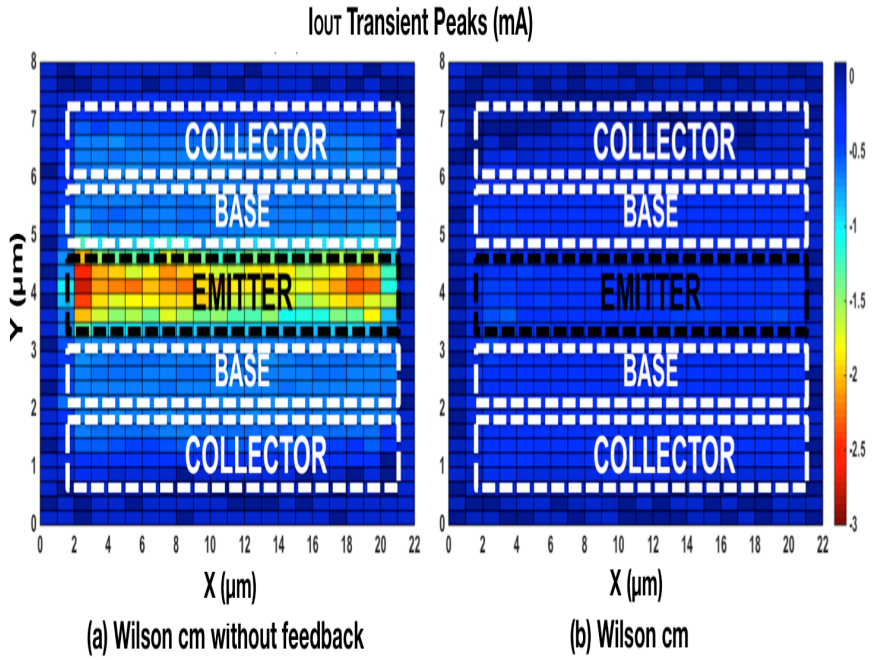


Fig. 6.11: 2-D raster scan plots show the peak output transient current as Q3 of Wilson current mirror with (a) and without (b) external feedback is impacted by the TPA laser.

A 2-D raster scan plot of the output device Q3 is shown in Fig. 6.11. The highest peak output transient current is reduced by 82% (from 2.7 mA to 0.5 mA) by the external negative feedback. The most sensitive area of the CBEBC NPN SiGe HBTs with respect to the laser strike is the emitter area, as illustrated in the 2-D raster scan plots, because the base-emitter and base-collector junction are located directly underneath the emitter contact, as illustrated in Fig. 6.12. As shown in the figure (blue arrow), the TPA laser penetrated the chips from their backside (p- substrate) to avoid the reflection by the metal lines on the topside of the circuit. The output transient current of the Wilson mirror and the Wilson mirror with external feedback removed, is plotted in the time domain (Fig. 6.13) as a fixed physical location on Q3 is struck by the laser. The peak transient of the Wilson current mirror is significantly lower than that of the Wilson mirror with feedback removed. The settling time of the Wilson mirror is shorter (i.e., faster recovery from a single event upset) than that of the Wilson mirror with feedback removed.

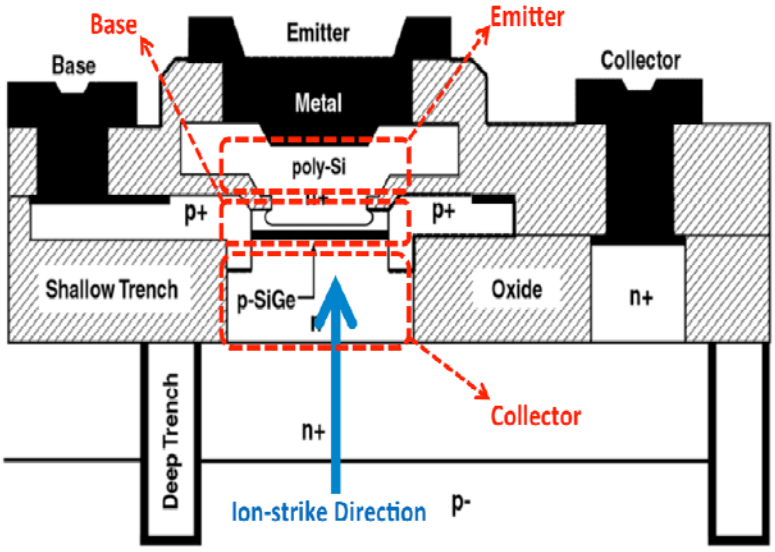


Fig. 6.12: The base-emitter and base-collector junctions, which are most sensitive with respect to the laser strike, are located directly underneath the emitter contact area. The TPA laser enters the chips from their backside, which is a p- substrate.

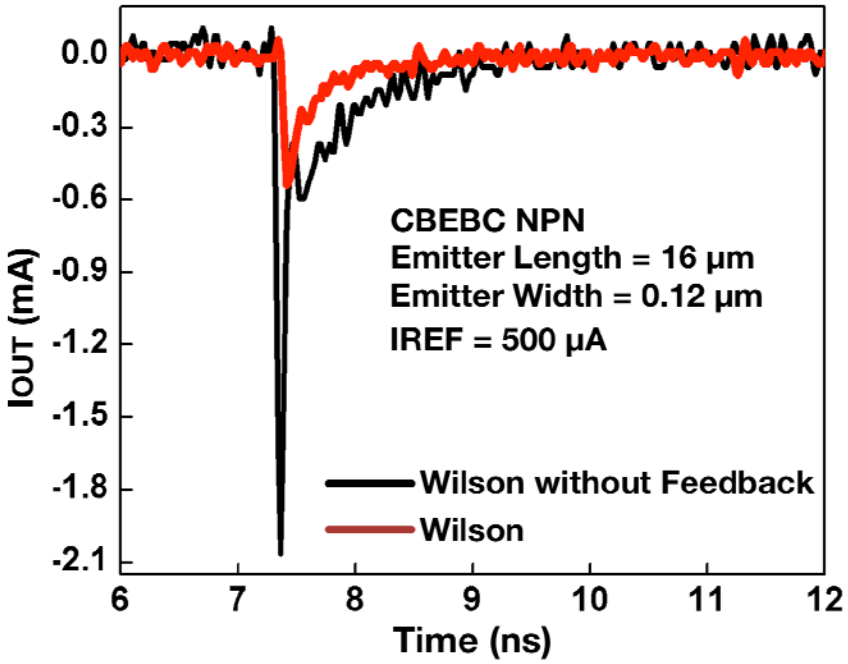


Fig. 6.13: The external negative feedback in the Wilson current mirror reduces the peak output transient current and recovery time as the output device Q3 is impacted by TPA laser.

6.7 Amount of Feedback

Equation (1) in section II predicts that if the amount of feedback ($1+A_1A_2\beta$) of a system increases, a single event transient in the output current can be reduced. According to equation (3), the amount of feedback in the basic common-emitter current mirror with emitter degeneration resistors increases as the value of its transconductance (g_m) and RE increases. In order to verify this, a 2-D mixed-mode TCAD model of 8HP SiGe HBTs was developed. After the model was calibrated to match the basic parameters of the transistor utilized in the current mirrors, it was used in mixed-mode (TCAD + circuit solved self-consistently) simulations of the basic common-emitter current mirror with and without RE. The RE values were set to 58, 86, and 115 Ω.

The purpose of this simulation is to verify the qualitative response of negative feedback. The main effort was made to match the percentage change between the peak

transient currents of the basic common-emitter current mirror with and without RE rather than the absolute magnitude from the measurement data. First, the calibrated model was used in a single-event transient simulation for the common-emitter current mirror without RE and with RE of 58 Ω (which is the actual value used in the fabrication of the mirror). As depicted in Fig. 6.14, the reduction by the internal feedback with RE = 58 Ω is close to the measured value, 50 %. An LET of about 1 MeV-cm^2/mg was used for the simulation.

Upon verifying that this simulation data is close to the actual measurement results, the emitter degeneration resistance value was increased to 86 and 115 Ω so as to increase the amount of feedback (based on (3)). The mixed-mode TCAD circuit simulation result in Fig. 6.15 confirms the prediction made by equation (1) and (3); that is, the larger the amount of feedback the lower the peak output transient current.

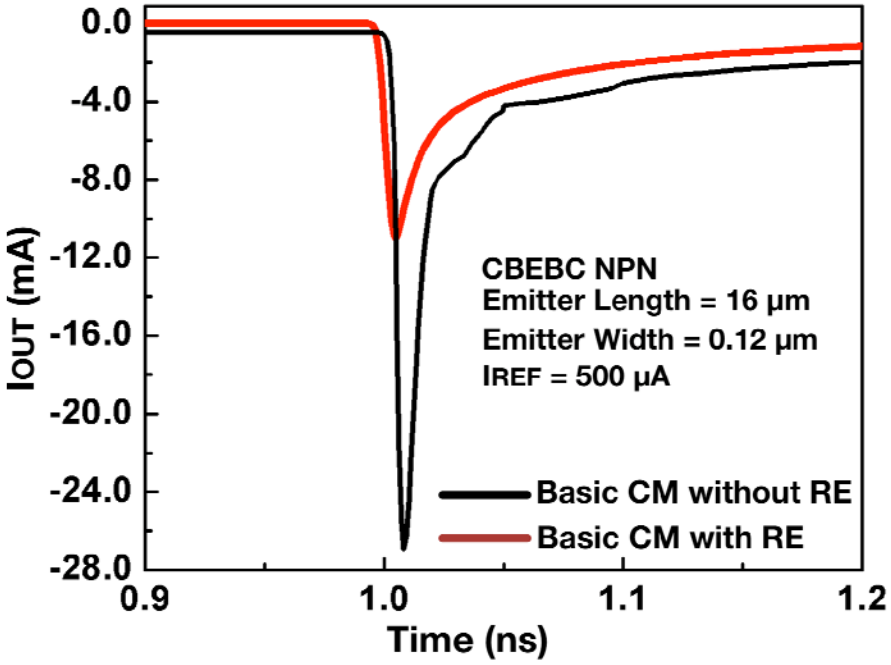


Fig. 6.14: Mixed-mode TCAD simulation result of the basic common-emitter current mirror with and without RE. RE is set to 58 Ω.

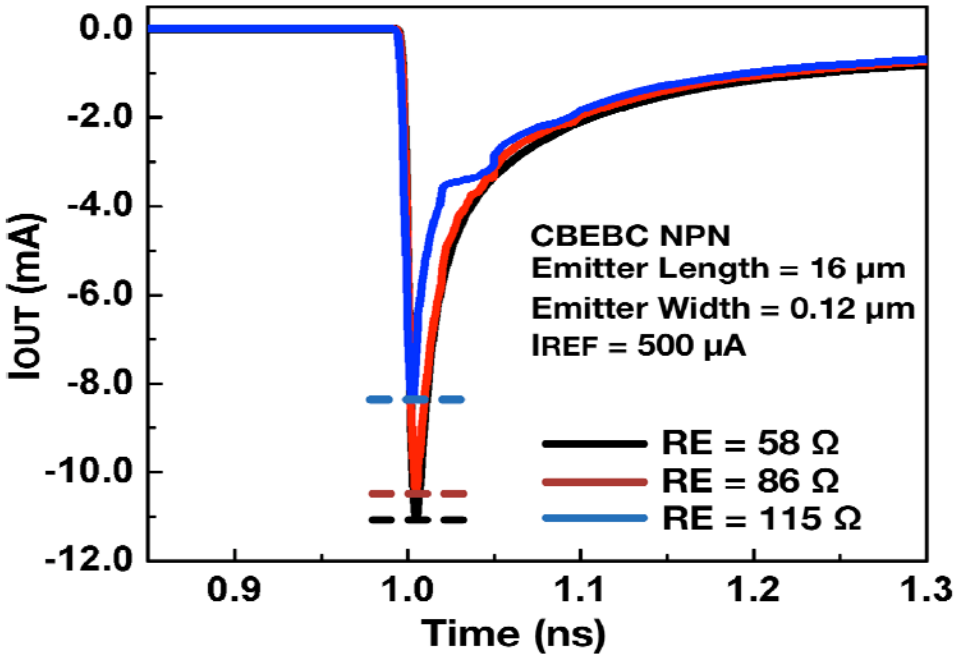


Fig. 6.15: Mixed-mode TCAD simulation result of the basic common-emitter current mirror with RE = 58, 86, and 115 Ω. The peak output transient current decreases as the amount of feedback ($1+A_1A_2\beta$) increases (i.e. RE value increases).

6.8 Discussion and Summary

The present work investigated internal and external negative feedback effects on single event transients in ubiquitous SiGe HBT analog circuits: current mirrors. Basic common-emitter NPN current mirrors, both with and without emitter degeneration resistors, were explored to study internal negative feedback effects. A simple addition of the emitter degeneration resistors in the basic common-emitter current mirror creates internal negative feedback and mitigates a single-event transient (SET). The highest peak output transient current is reduced by 50%, and the settling time of the output current upon a TPA laser strike is shortened with internal negative feedback. The supply voltage (V_{CC}) influence on a single event transient was investigated as well. The peak output transient current increases as the supply voltage increases due to the extra electron-hole pairs generated by avalanche.

A Wilson current mirror was also investigated to look into external feedback effects on single event transients. A Wilson mirror and a Wilson mirror with its intrinsic external negative feedback removed were explored, and their response to a single event was recorded and analyzed. The highest peak output transient current is reduced by 82% when the output device Q3 is struck by the TPA laser, and the settling time of the output current upon a laser strike is shortened with external negative feedback. The inversely proportional relationship between the amount of feedback and the peak output transient current was verified utilizing mixed-mode TCAD circuit simulations. A 2-D model for the transistor used in all four current mirrors was developed by closely matching the basic parameters of the transistor.

The main drawback associated with introducing negative feedback in a circuit is that the feedback reduces sensitivity of large-signal high-speed circuits such as comparators. For instance, placing internal negative feedback by adding emitter degeneration resistors in a differential common-emitter transistor pair of an ECL high-speed comparator reduces the sensitivity of the comparator (i.e., its output response to the changes in the input becomes slower).

The sensitivity of the simple differential comparator with emitter degeneration resistors as shown in Fig. 6.16 can be expressed in terms of the effective transconductance (G_m) of the differential pair Q1 and Q2, which determines the gain of the comparator. The effective transconductance G_m is given as

$$G_m = \frac{1}{2(r_e + RE)} \tag{9}$$

where $r_e = V_T / I_E$; V_T is the thermal voltage and I_E is the DC emitter current. As illustrated in the equation, RE that creates an internal negative feedback decreases the sensitivity of the comparator. For example, the effective transconductance G_m decreases

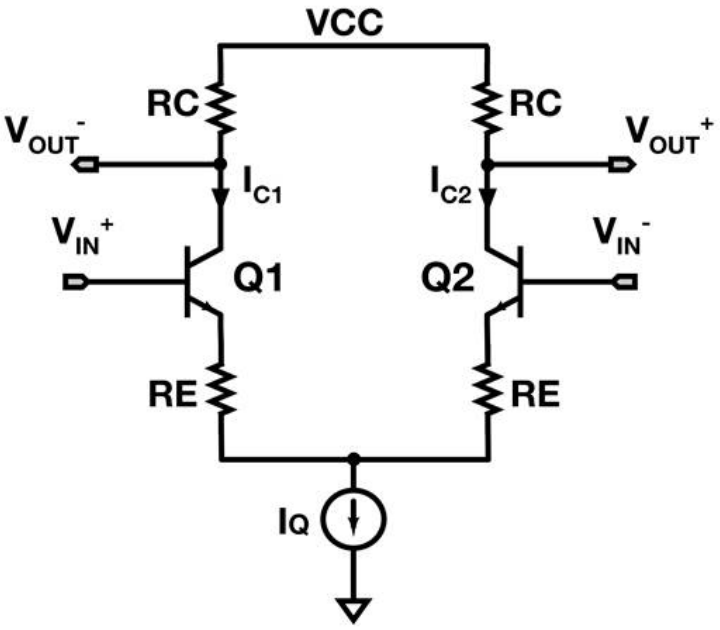


Fig. 6.16: Comparator composed of a differential pair with emitter degeneration resistor RE.

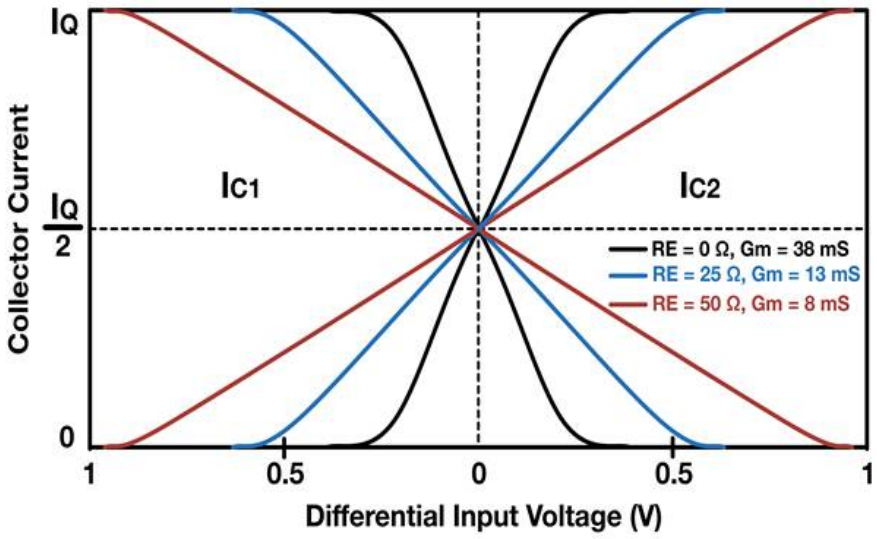


Fig. 6.17: Collector current versus differential input voltage (V_{IN}^+ - V_{IN}^-) of the comparator in Fig. 6.16. The sensitivity of the comparator (the slope of the collector current) decreases as RE increases.

from 38 to 13 and to 8 *mS* as the RE value increases from 0 to 25 and to 50 Ω at I_Q = 4 mA assuming room temperature (i.e. $V_T \approx 26$ mV). Hence the sensitivity of the comparator decreases as the amount of feedback increases (or RE increases). The collector current versus differential input voltage ($V_{IN}^+ - V_{IN}^-$) of the comparator is also plotted in Fig. 6.17. The slope of I_C represents the effective transconductance G_m of the differential pair. As depicted in the plot, the sensitivity of the comparator (the slope of I_C) decreases as the degeneration resistor RE increases.

All SiGe HBTs in the investigated current mirrors showed their most acute response when their emitter region was struck by the TPA laser. This makes sense, because the base-emitter and base-collector junction, which are most sensitive region in a HBT with respect to a single event strike, are located underneath the emitter contact area.

6.9 Considerations for Future Work

Although the external feedback is broken at the highest impedance node in the Wilson current mirror, which is a common practice for feedback analysis, it is desirable to incorporate physical loading effects seen looking out of the base of Q3 and collector of Q1 in Fig. 6.4 (b) into the test bench in order to attain a more accurate picture of its single-event response.

The observations and analysis made on internal and external negative feedback in this work can be applied to circuits with a negative feedback whose loop-gain is greater than unity. However, experimental validation of the feedback effects in more complex circuits such as operational amplifiers is in progress in order to strengthen the reliability of the findings made here.

6.10 Acknowledgement

This work was supported by the Defense Threat Reduction Agency under contract HDTRA1-13-C-0058. Seungwoo Jung would like to graciously thank IBM for access to their 8HP SiGe BiCMOS technology.

CHAPTER 7

HIGH-SPEED FLASH ANALOG TO DIGITAL CONVERTER FOR RECEIVER CHAINS OF RADAR SYSTEMS

7.1 High-Speed Flash ADC for a Radar Receiver

The diagram in Fig. 7.1 depicts a conventional radar system. The receiver module, mixer, and baseband module in the receiver chain add complexity and delay to the receiver path. Fig. 7.2 shows the same radar system with an ADC replacing the receiver module, mixer, and baseband module. The diagram clearly illustrates how significantly the ADC can simplify the receiver chain of the radar system. In this way, the time delay between the antenna and the baseband system can be reduced profoundly, and, as a result, the radar system can operate in closer proximity of the true time domain. As the operating frequency of radar systems increases, ADCs need to be designed utilizing a fast (high f_T) process. A 5-bit flash ADC is designed to replace receiver chain components (except the LNA) of a phased array radar system whose input spectrum ranges from DC to 12 GHz (up to X-band) utilizing IBM 8HP SiGe BiCMOS technology with the peak f_T of 220 GHz. Each channel of the flash ADC consists of a high-speed comparator cascaded with a high-speed D flip-flop. The radiation hardening by design technique discussed in Chapter 6 (internal negative feedback) is applied to the sub-analog components (high-speed comparator, high-speed D flip-flop) of the ADC to reduce single-event effects.

7.2 High-Speed Comparator

Fig. 7.3 shows the high-speed comparator. It consists of three gain stages to ensure the output of the comparator is either voltage high or low (i.e., logic high or logic low). The first stage employs two cross-coupled fully differential pairs to receive the

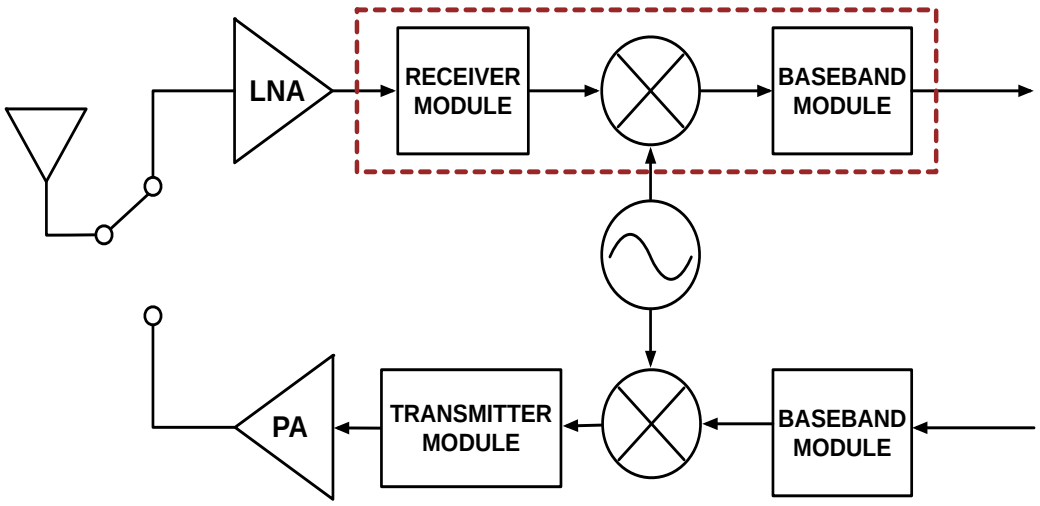


Fig. 7.1: Conventional radar system with receiver and transmitter chains.

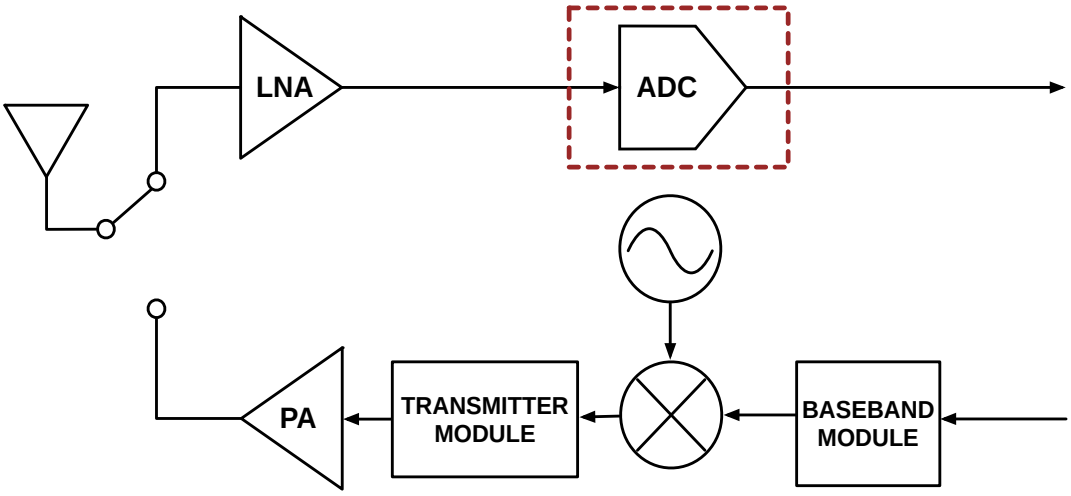


Fig. 7.2: Receive chain (except LNA) is replaced with an ADC.

differential reference voltages (VREF+ and VREF-). The second and third stages are composed of a fully differential emitter-coupled logic (ECL) pair and a fully differential cascode amplifier, respectively, to further boost the overall voltage gain. The cascode configuration is utilized in the last gain stage in order to increase the output resistance and isolation. Emitter follower buffer stages are placed between the gain stages to separate them from each other.

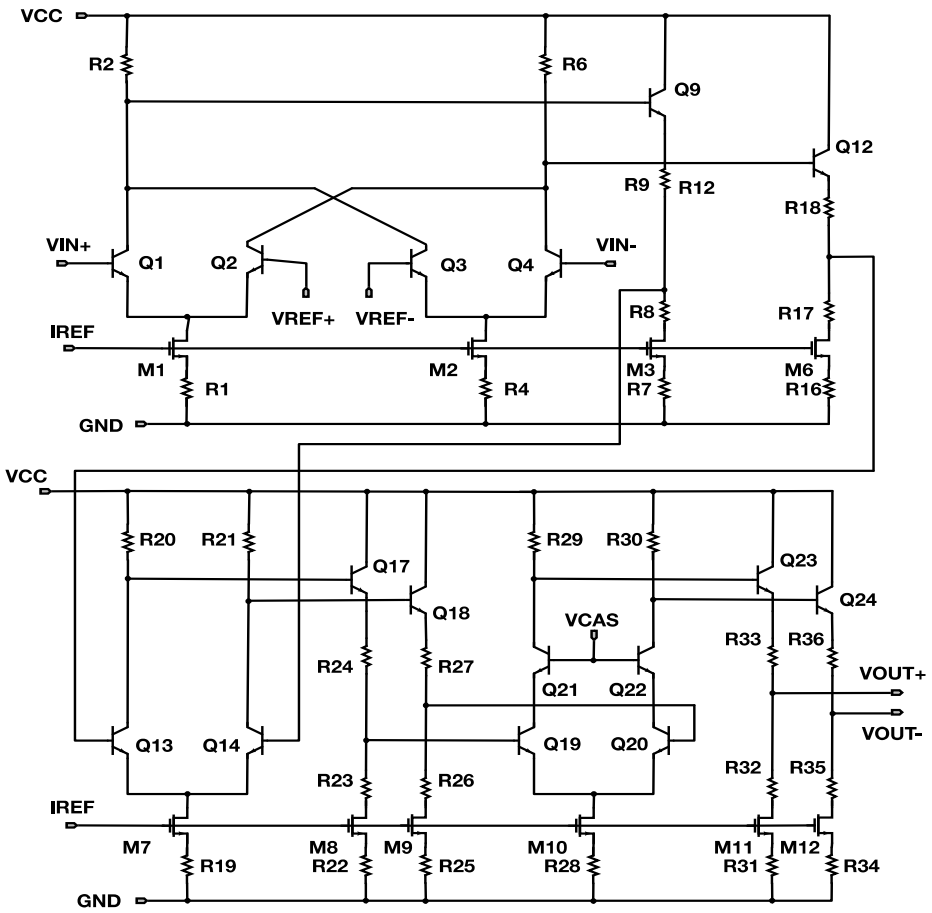


Fig. 7.3: Three gain-stage high-speed comparator.

A source degeneration resistor that forms an internal negative feedback is added to all the current mirrors in order to reduce a peak transient response in the mirrors based on the findings made in Chapter 6; i.e., the internal negative feedback helps the DC bias condition to recover its original state from a disturbance caused by a single-event. The comparator in Fig. 7.3 and an identical comparator with the source degeneration resistors removed have been taped out utilizing IBM 8HP for the purpose of single-event radiation testing.

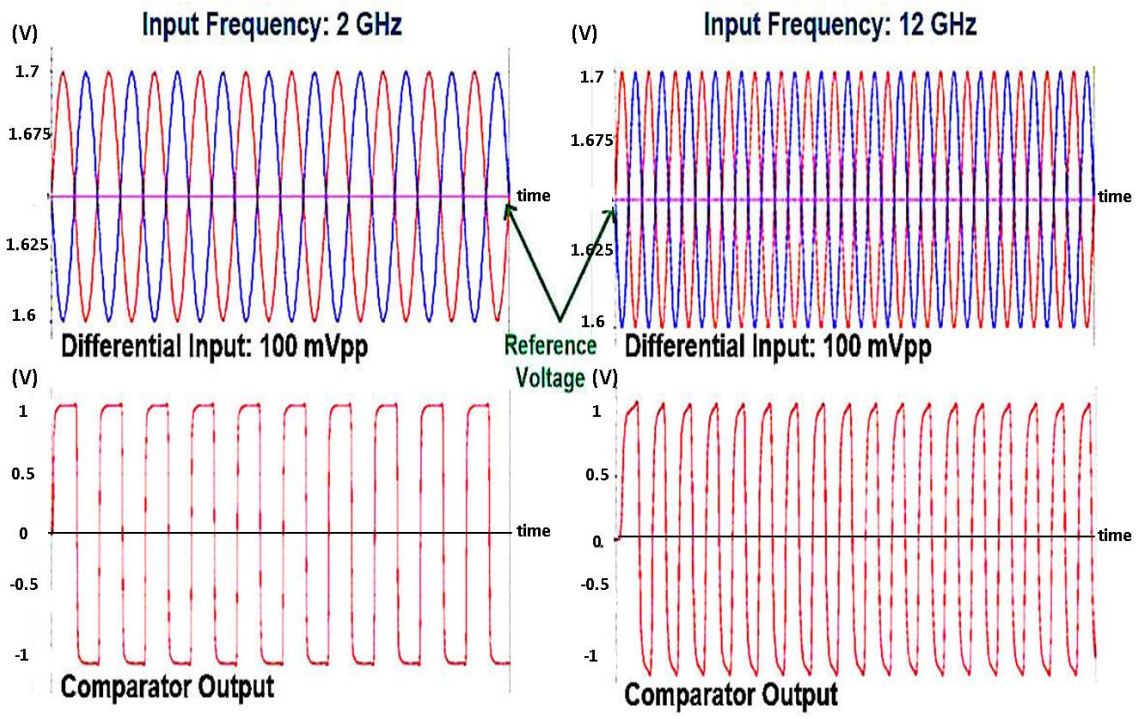


Fig. 7.4: Cadence transient simulation result of comparator at input frequency of 2 and 12 GHz.

The simulation results of an independent comparator at 2 and 12 GHz input are shown in Fig. 7.4. The output voltage swing of 2 V_{pp} at both the input frequencies of 2 and 12 GHz demonstrates that the comparator is capable of operating at 12 GHz. A

comparator array that consists of 31 comparators (5-bit) in parallel also simulated with reference ladders that generate 31 voltage references, and the result is shown in Fig. 7.5. The input voltage swing and frequency are set at 1 V_{pp} and 10 GHz, respectively. As shown in the figure, the comparator array misses only the first LSB.

The die photo and layout of the comparator are shown in Fig. 7.6. All active components (HBT and MOS devices) are closely placed to each other in order to minimize the effects of parasitic components. In addition, the circuit components are laid out in a symmetrical manner as shown in Fig. 7.6 (b).

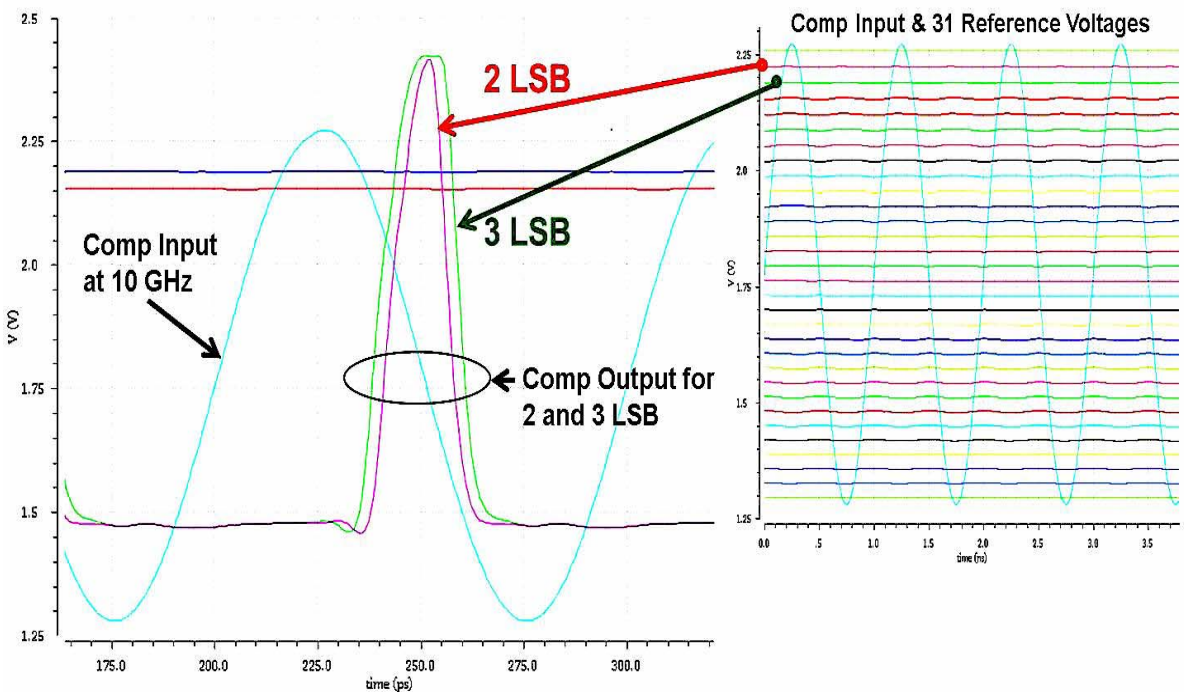


Fig. 7.5: Cadence transient simulation result of a comparator array (31 comparators) with differential resistor ladders.

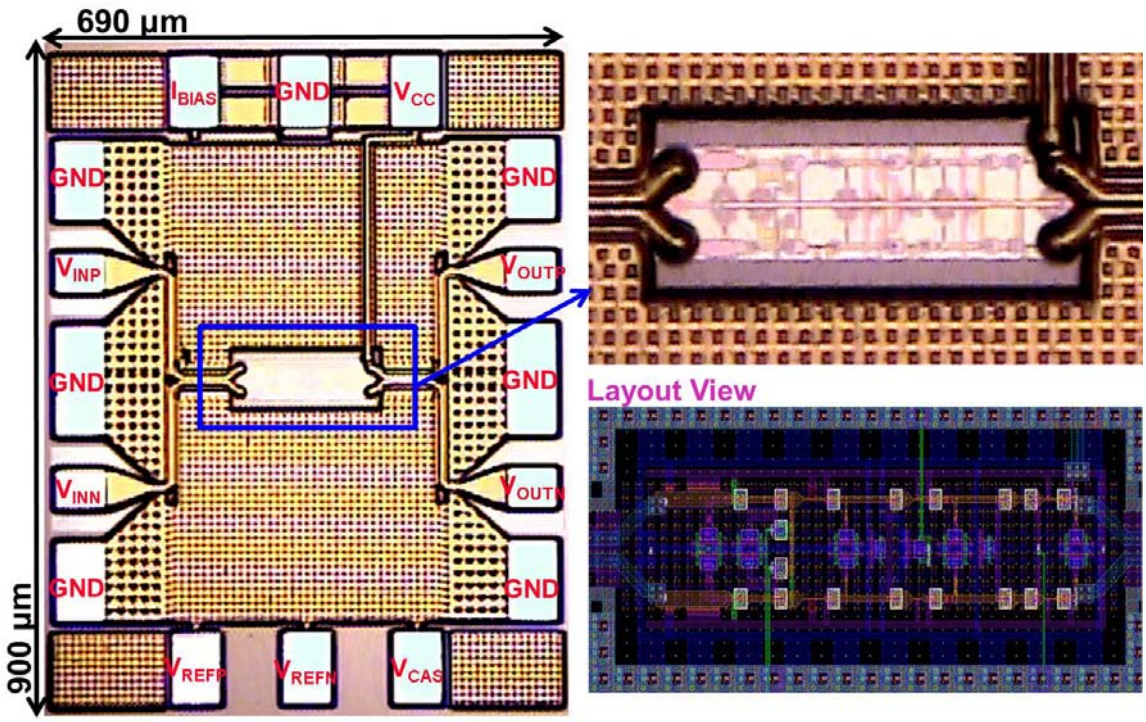


Fig. 7.6: Layout of high-speed comparator.

7.3 High-Speed D Flip-Flop

The D flip-flop that samples the incoming data according to the clock signal employs ECL logic to achieve high-speed operation; since the maximum frequency of the input data is 12 GHz, the sampling frequency needs to be greater or at least equal to its Nyquist rate, which is 24 GHz.

Fig. 7.7 shows the high-speed ECL D flip-flop. It is composed of two high-speed latches with positive feedback loops. The positive feedback loops enhance latching capability of the circuit. The differential clock signals (CLK+ and CLK-) are cross-coupled between the two latches. When CLK+ is high, and CLK- is low (Q1 and Q10 are on, Q2 and Q9 are off), the first latch samples the input, and the second latch puts out the previously latched value. When CLK+ turns low, and CLK- turns high (Q1 and Q10 are

off, Q2 and Q9 are on), the first latch latches the input and passes the value to the next latch.

A source degeneration resistor is added to all the current mirrors, and an emitter degeneration resistor is added to all differential pairs (Q3-Q4, Q5-Q6, Q11-Q12, and Q13-Q14) in the AC input path. These source and emitter degeneration resistors form an internal negative feedback and reduce a peak transient response based on the findings made in Chapter 6. The D flip-flop in Fig. 7.7 and a structurally identical D flip-flop with the source and emitter degeneration resistors removed have been taped out utilizing IBM 8HP for the purpose of single-event radiation testing.

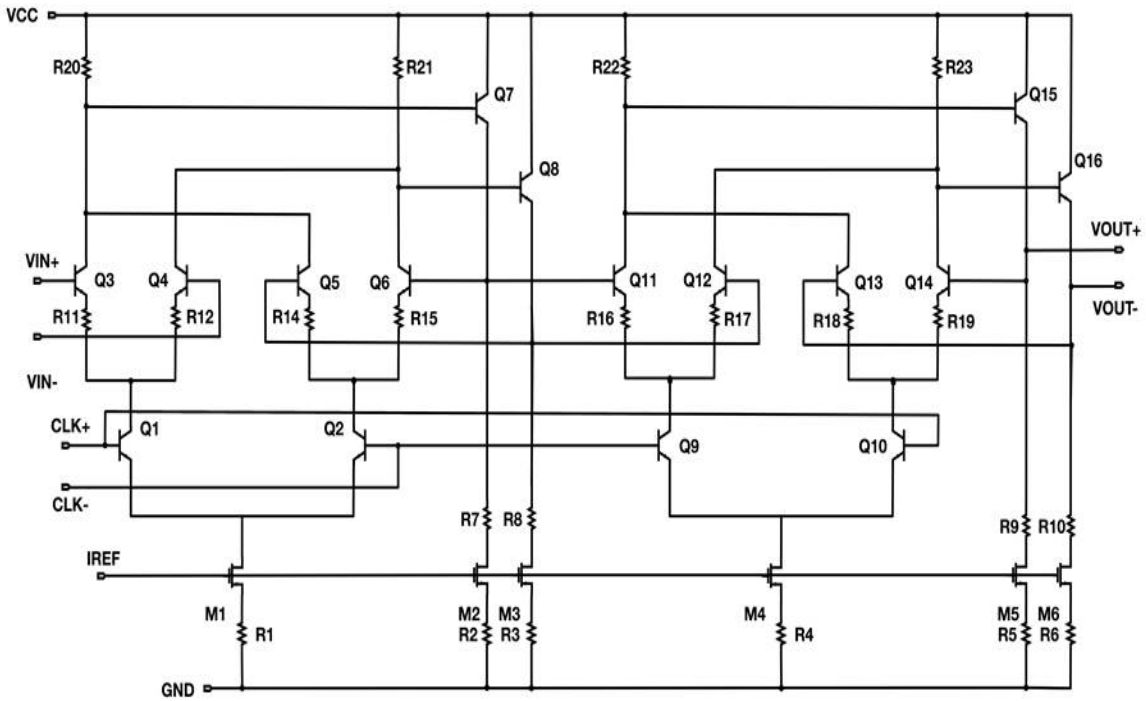


Fig. 7.7: High-speed D flip-flop.

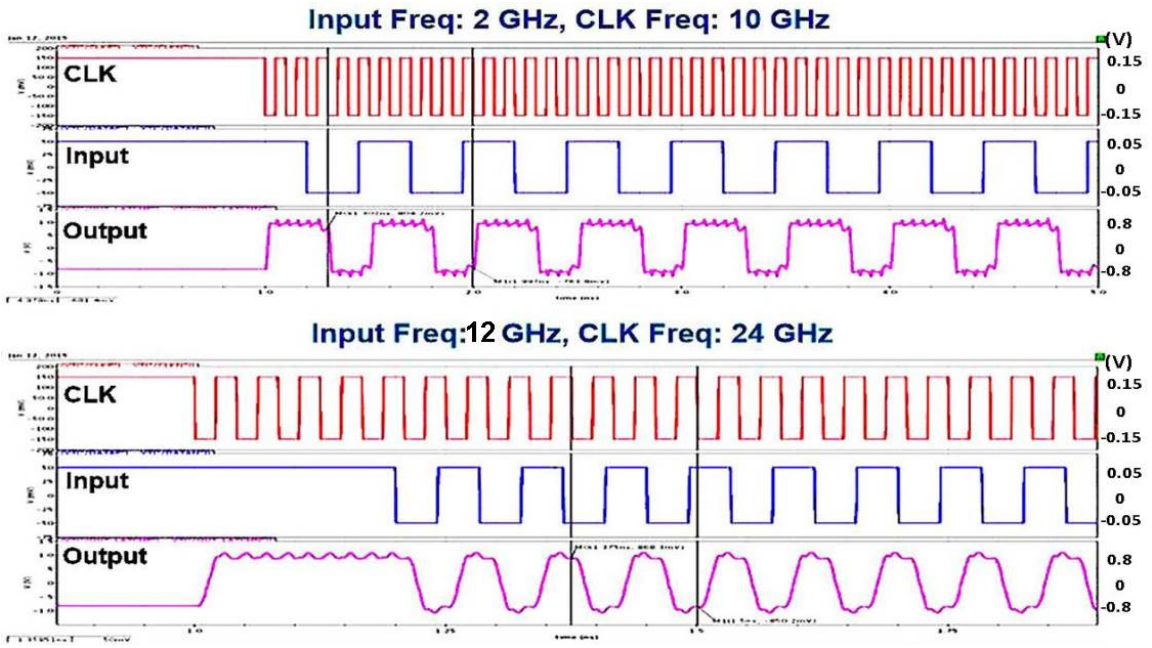


Fig. 7.8: Cadence transient simulation result of high-speed D flip-flop.

The top plot of Fig. 7.8 shows the transient simulation result of the D flip-flop with the input signal at 2 GHz and the CLK signal at 10 GHz. The simulation result with the input signal at 12 GHz and the CLK signal at 24 GHz (Nyquist Frequency) is also shown in the bottom plot. The results demonstrate that the D flip-flop is capable of operating at the input of 12 GHz with a sampling rate of 24 GHz (Nyquist rate).

The die photo and layout of the D flip-flop is shown in Fig. 7.9. All active components (HBT and MOS devices) are closely placed to each other in order to minimize the effects of parasitic components. In addition, the circuit components are laid out in a symmetrical manner as shown in Fig. 7.9 (b).

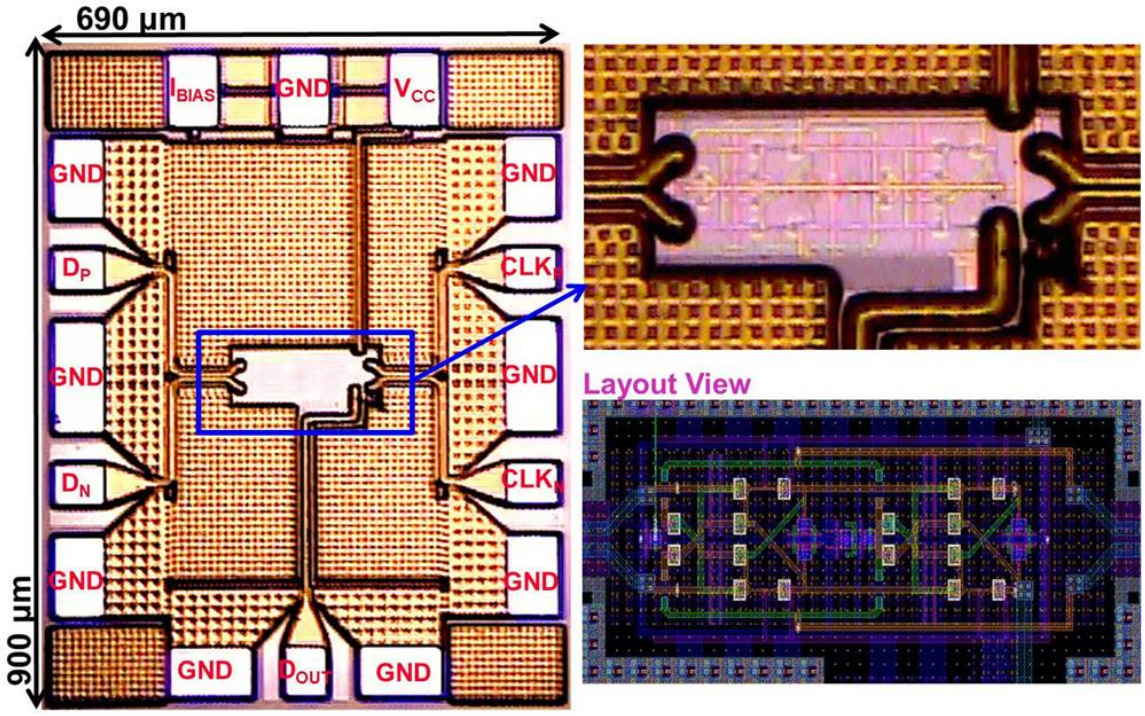


Fig. 7.9: Layout of high-speed D flip-flop.

7.4 5-Bit High-Speed Flash ADC

The 5-bit (31-channel) flash ADC system is shown in Fig. 7.10. Each channel of ADC consists of a high-speed comparator, a high-speed D flip-flop, and buffers. Each comparator takes differential reference voltages from the resistor ladders and compares the reference voltages with the incoming differential data signal. The differential reference voltages are generated by voltage division of V_{REFP} and V_{REFN} through the resistor ladders. The output of each comparator (either voltage high or low), then, is fed to a high-speed D flip-flop. An array of D flip-flops samples the incoming signal from the output of each comparator based on differential clock signals. The output values of the D flip-flop array are transferred to a decoder and converted as a digital value.

Since the base current of a SiGe HBT is non-zero (hence finite base impedance), buffers are required to drive the comparators and D flip-flops. Buffers utilize an emitter follower so that they can supply a non-zero base current without disturbing DC bias of the circuit. In addition, they provide a good isolation between stages.

In order to test this high-speed ADC, a high-speed thermometer Digital to Analog Converter (DAC) is also designed (Fig. 7.11). The DAC employs the current steering scheme. The 31 HBT differential pairs in the DAC take thermometer data (output of the D flip-flop array) from the ADC. Based on this incoming data (either voltage high or low), only one HBT device from a differential pair turns on, and all current flows through that device. Collectors of all 31 HBT differential pairs are tied together to two 50 Ω resistors as shown in Fig. 7.11 so that the summed total collector current can be converted to a voltage. The value of 50 Ω is chosen to match the transmission line impedance. The cadence transient simulation results are shown in Fig. 7.12 and Fig. 7.13. An input sinusoidal voltage wave at 1 GHz is passed to an ideal 5-bit ADC with a sampling frequency of 20 GHz, and its thermometer output codes are fed to the DAC in Fig. 7.12. The DAC reconstructs the input sinusoidal at its output. The quantization noise is caused by the limited resolution (5-bit); i.e., if the resolution is not limited, an ideal DAC puts out an identical sinewave to the original input signal. The DAC is also tested with an input sinusoidal voltage wave at 10 GHz with an ADC (ideal) sampling rate of 20 GHz (Nyquist rate) as shown in Fig. 7.13.

The output of the ADC is directly connected to the input of the DAC as shown in Fig. 7.14 (red-dotted box) in order to investigate the ADC's performance. Since the ADC and DAC are cascaded directly, theoretically, the frequency of an input sinusoidal voltage wave is to be the fundamental frequency in the output signal of the DAC. The simulation

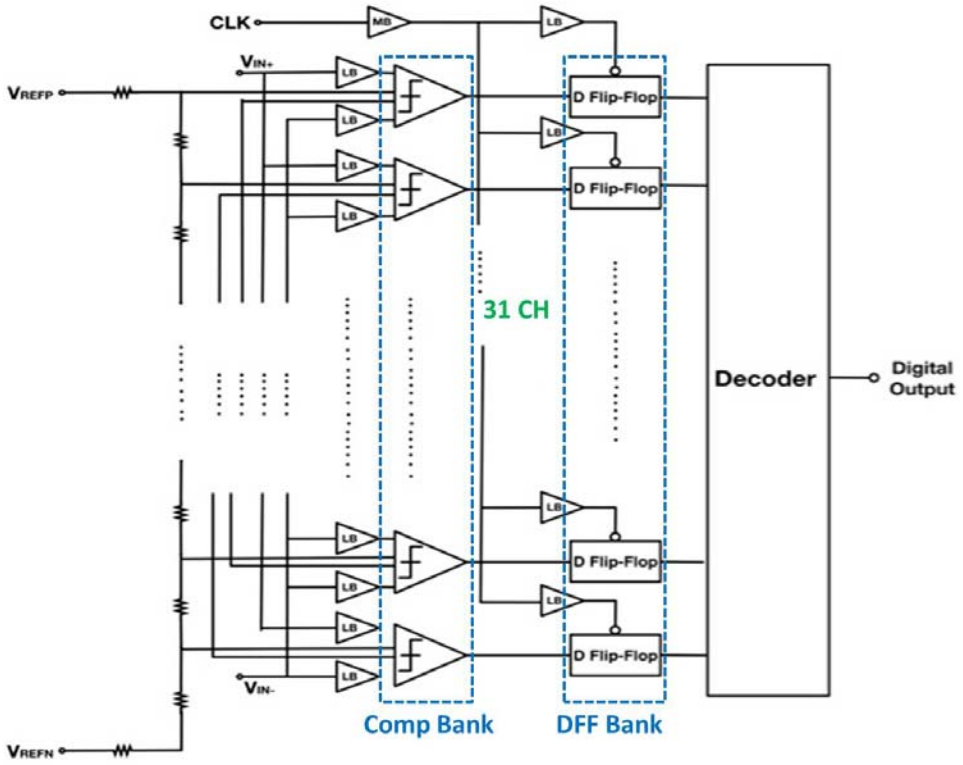


Fig. 7.10: 5-bit (31-channel) high speed flash ADC.

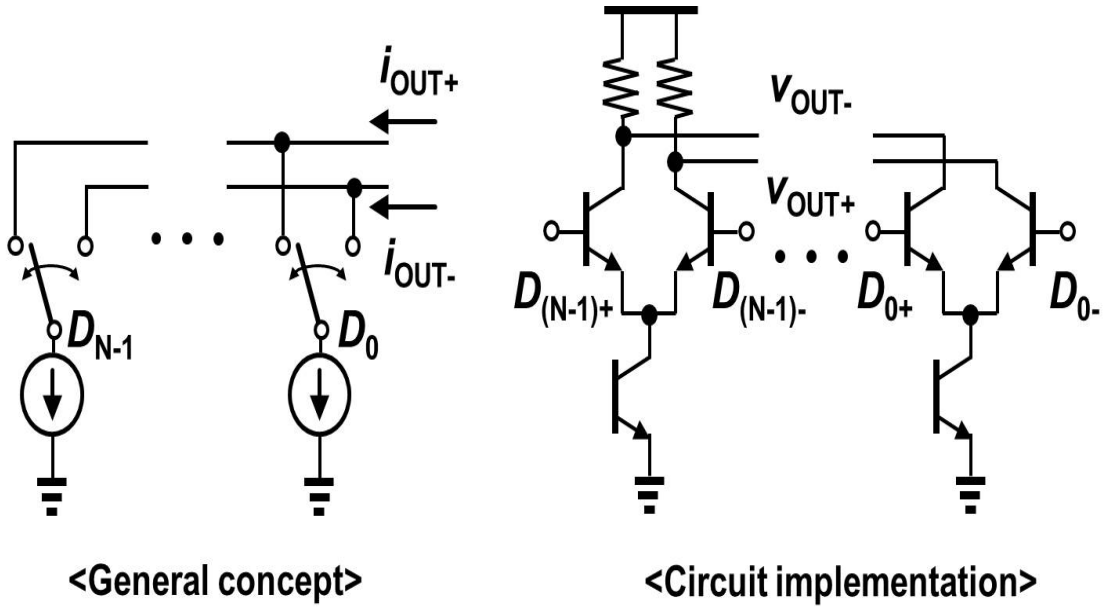


Fig. 7.11: High-speed current steering thermometer DAC.

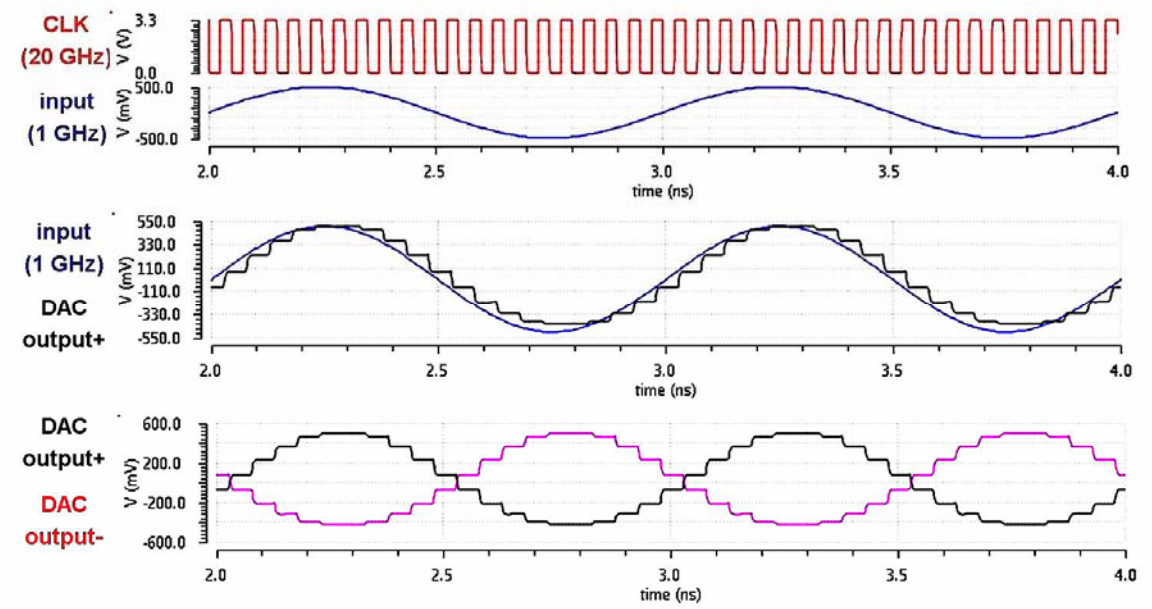


Fig. 7.12: Cadence transient simulation result of DAC with sinusoidal input at 1 GHz.

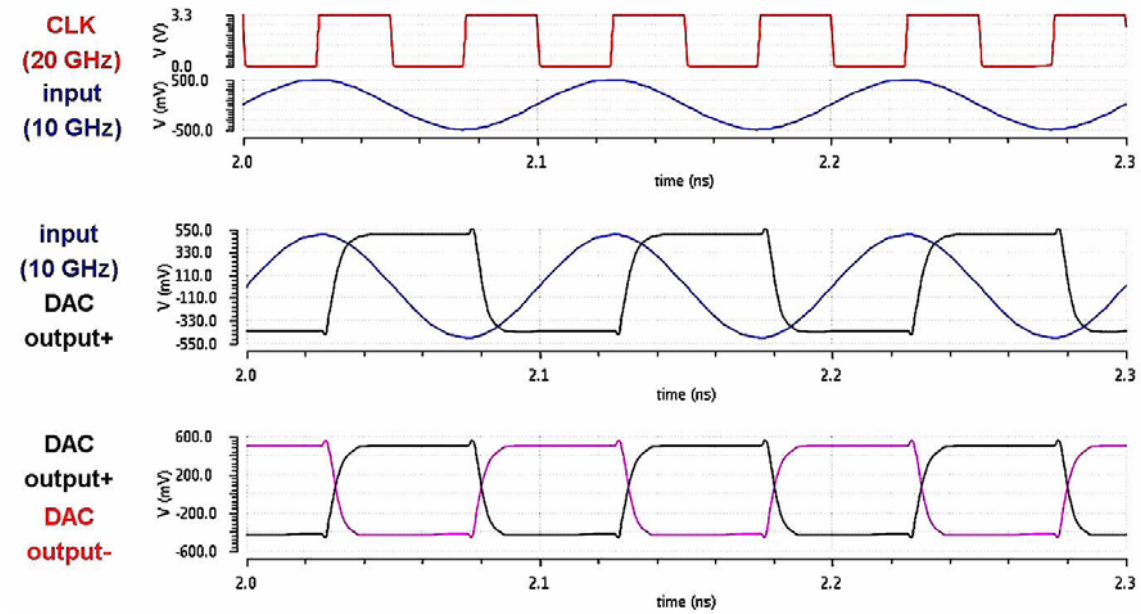


Fig. 7.13: Cadence transient simulation result of DAC with sinusoidal input at 10 GHz.

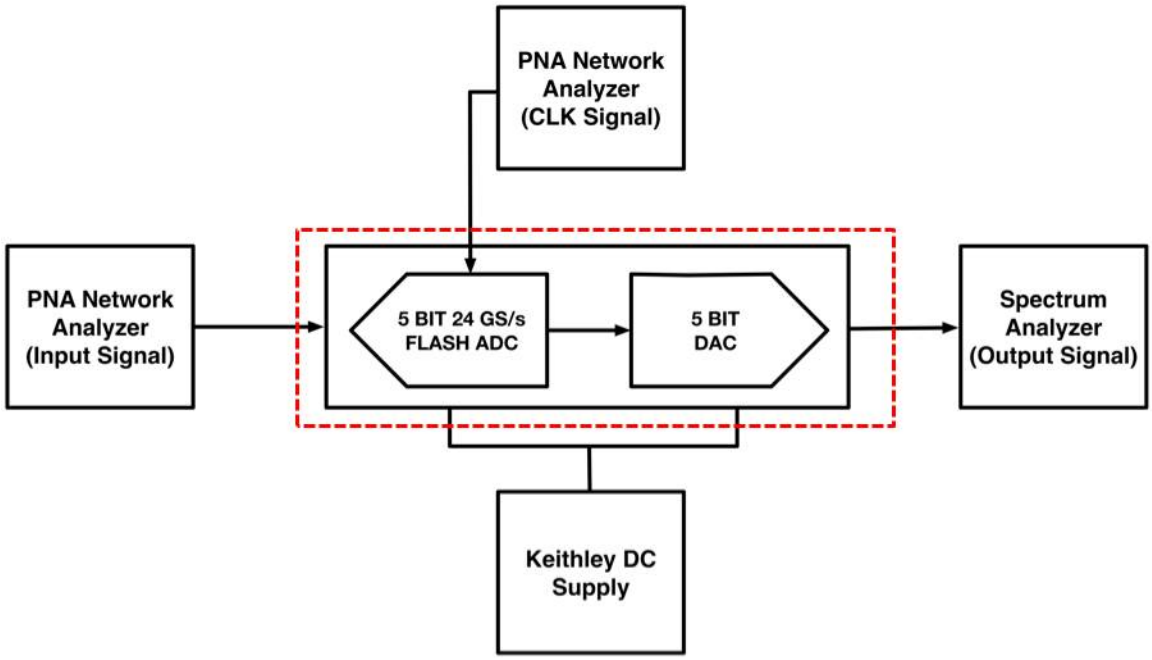


Fig. 7.14: ADC and DAC test bench.

results of the ADC and DAC connected together with an input signal at 10 GHz and sampling (clock) signal at 20 GHz (Nyquist rate) is shown in Fig. 7.15. The ADC is simulated with the thermometer DAC. There are overshoots in the output of the thermometer DAC because the output voltage level of the ADC is not as flat as those of ideal ADC as shown earlier in Fig. 7.8. The thermometer DAC output can be measured by either a real-time high-speed oscilloscope or spectrum analyzer. An input and clock signal for the ADC can be generated by two high-frequency network analyzers (Fig. 7.14). The simulated specifications of the ADC are listed in Table 7.1.

The top view of the ADC and DAC layout is shown in Fig. 7.16. The die size is 5.6 mm x 2 mm. All top routing metal lines are EM simulated utilizing Sonnet EM simulator to ensure their characteristic impedance stays close to 50 Ω over the bandwidth of interest. The optimal width of the top metal is decided to be 6 μm based on the EM

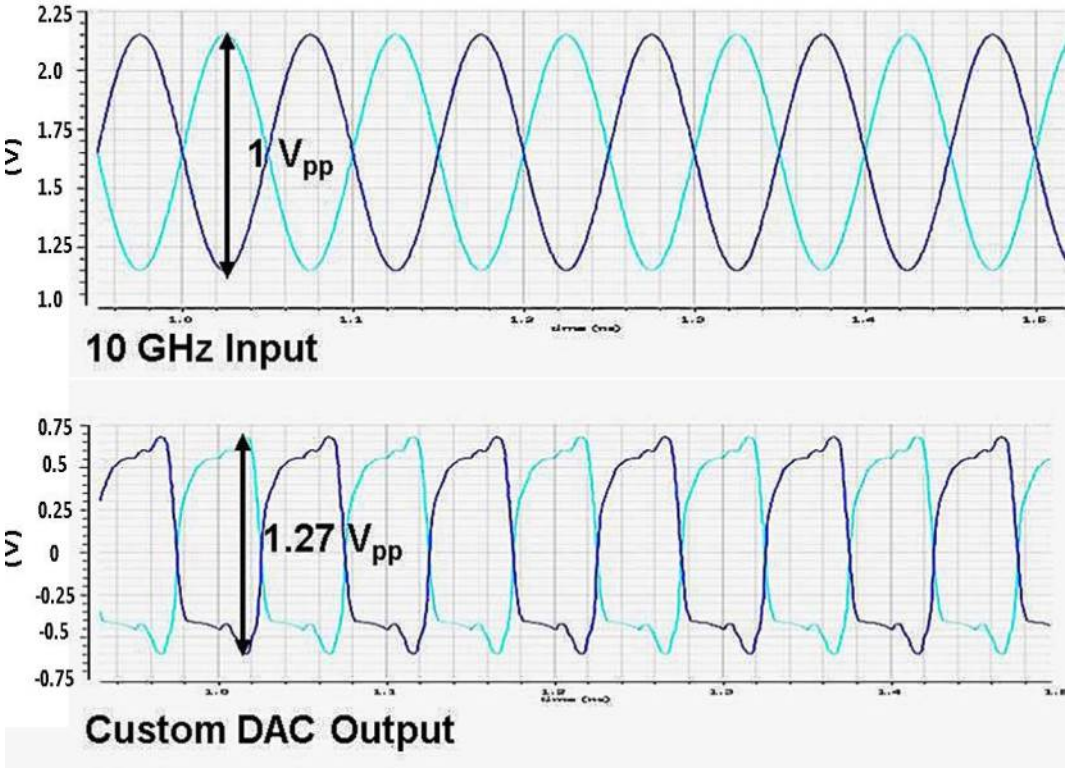


Fig. 7.15: Cadence transient simulation of ADC and DAC together (Fig. 7.14).

Table 7.1: ADC Simulated Specifications.

Specs	Simulated Values
Technology f_T (IBM 8HP)	220
Sampling rate (GHz)	20
Nyquist Frequency (GHz)	20
Resolution / bits	5
ENOB @ Nyquist Rate	3.5
SFDR (dB)	33.2
SNDR (dB)	22.5
Power (W)	3

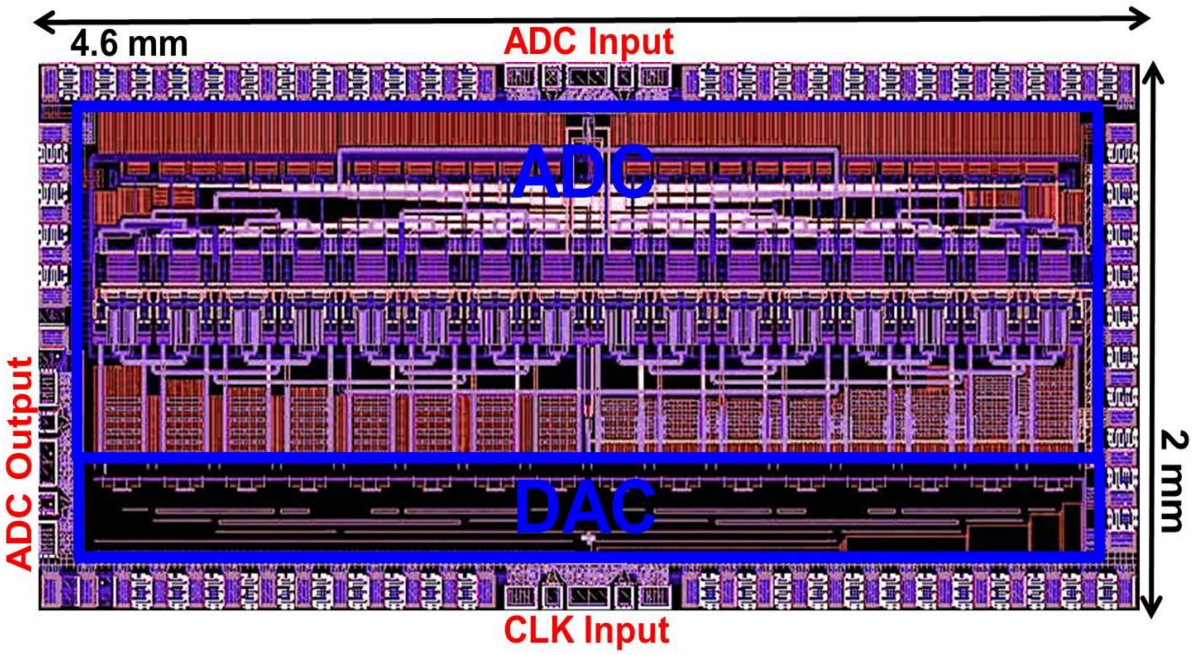


Fig. 7.16: Top view of ADC and DAC layout.

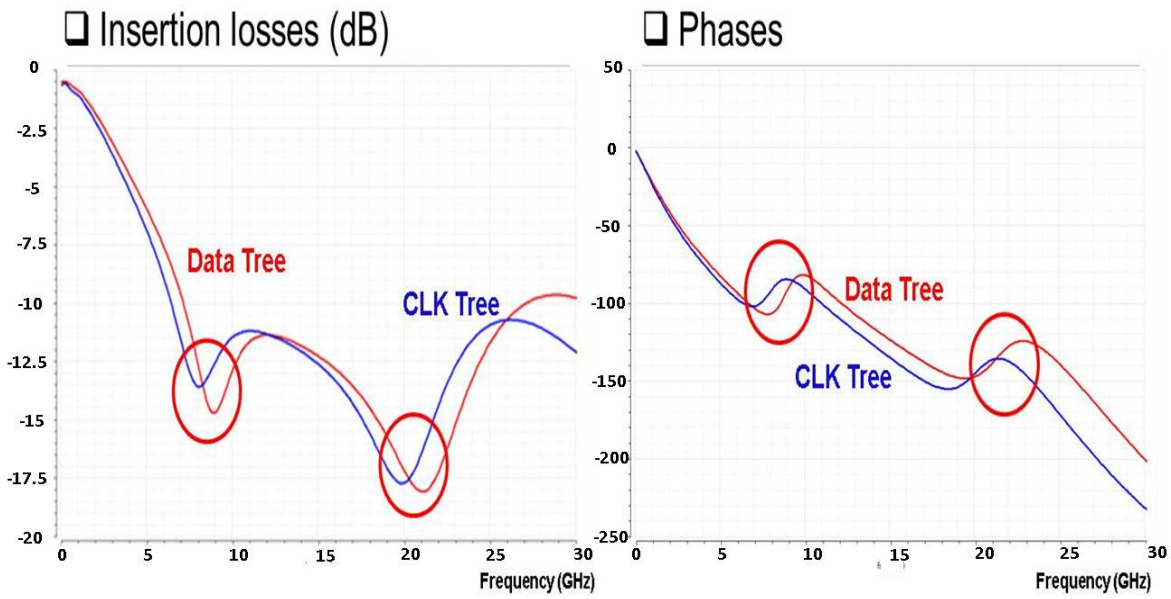


Fig. 7.17: EM simulation results for insertion loss and phase response of data and clock line.

simulation results. Fig. 7.17 shows the EM simulation results for insertion loss and phase response of the top metal line. As shown in the figure, the insertion loss and phase are closely matched between the data lines and clock lines over the frequency range from DC to 30 GHz. The input data and clock signal lines are laid out in a tree configuration to match the electrical length of all channels as illustrated in Fig. 7.18 [64]-[66].

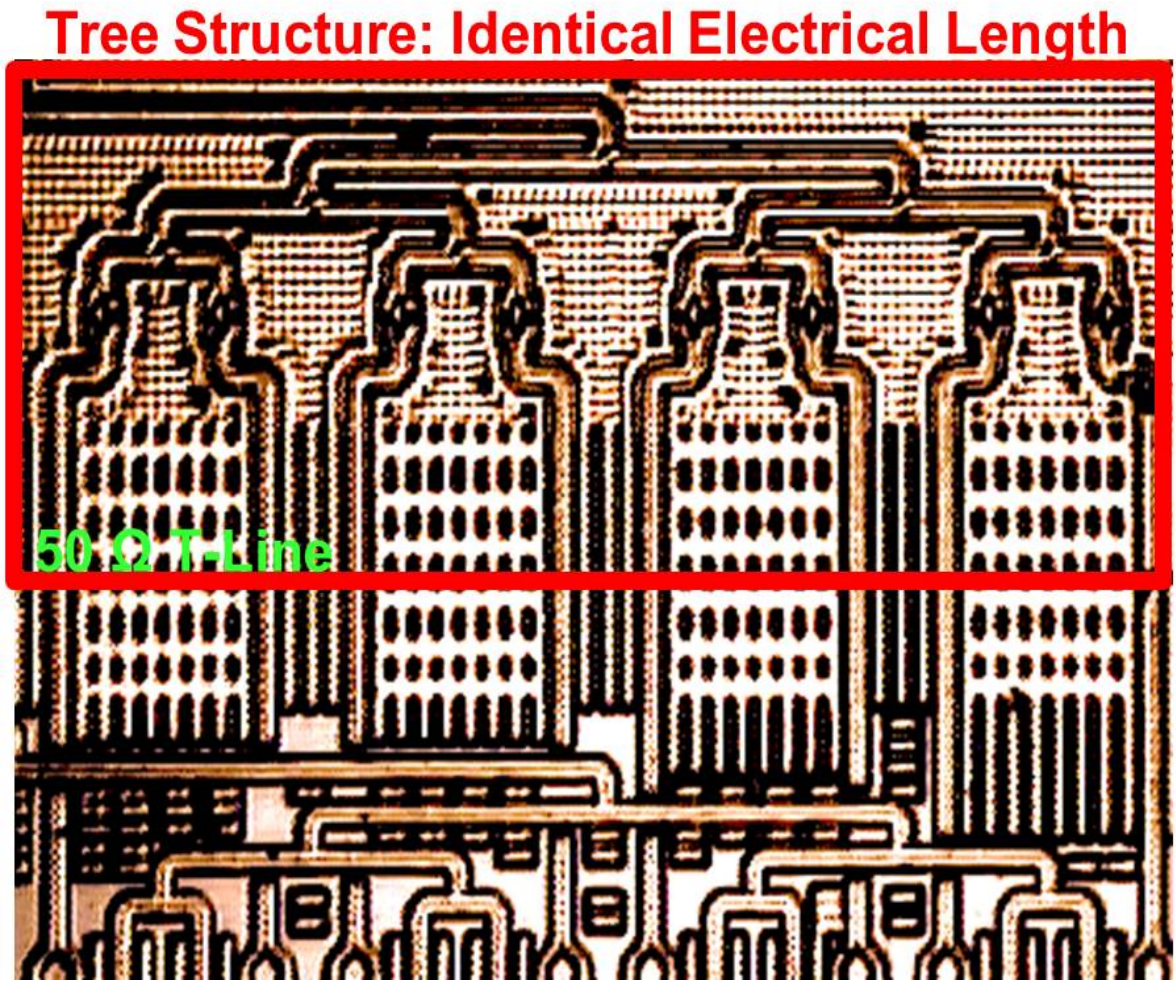


Fig. 7.18: Tree configuration of data and clock lines to match the electrical length of all channels.

7.5 *Single-Event Transient (SET) Response on ECL Circuit*

The core building block of both the comparator and D flip-flop is the high-speed ECL circuit. The ECL circuit consists of two main parts as shown in Fig. 7.19: AC differential circuit and DC current source (or DC current mirror).

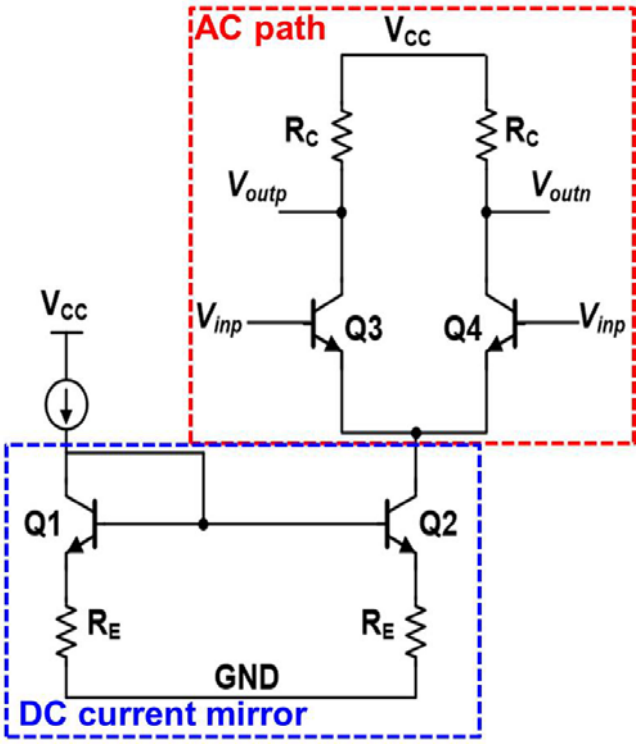


Fig. 7.19: Emitter-coupled logic (ECL) circuit consists of AD differential pair and DC current source (or DC current mirror).

It has been shown earlier that negative feedback can improve SET response in DC current mirrors; the peak transient was reduced, and the settling time was shortened. In this section, effects of the radiation hardening techniques applied in DC current mirrors (including internal negative feedback) on the ECL AC differential circuit (i.e., AC signal path) are investigated.

The radiation hardening techniques applied in DC current mirrors are combinations of internal negative feedback (R_E) and the capacitor (C) connected between the base of the reference device and ground as depicted in Fig. 7.20: $R_E = 0\ \Omega$ and C = 0, $R_E = 100\ \Omega$ and C = 0 F, $R_E = 0\ \Omega$ and C = 12 pF, $R_E = 100\ \Omega$ and C = 12 pF.

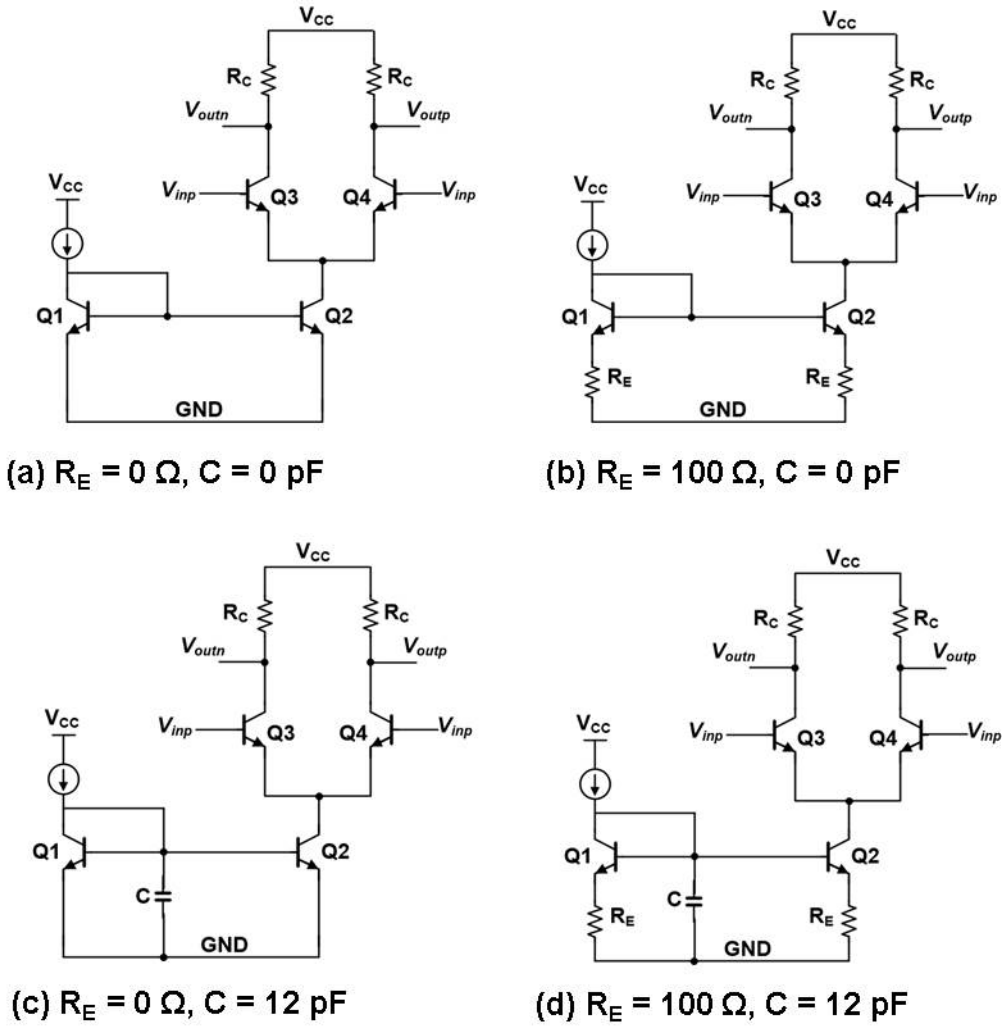


Fig. 7.20: Radiation hardening techniques in DC current mirrors utilizing internal negative feedback (R_E) or/and a capacitor (C).

The output transistor Q2 of the current mirrors of all four ECL circuits in Fig. 7.20 is struck by the TPA laser, and the transient responses at the inverting output terminal are measured. The internal negative feedback created by R_E (100 Ω), as expected, improves the SET response of the current mirror output; i.e., the peak transient of the inverting output voltage (solid blue line in Fig. 21) is reduced. The capacitor (12 pF) connected between the base of the reference device (Q1) and ground reduces the output peak transient of the current mirror as well (dotted magenta line in Fig. 21) because the voltage across the capacitor cannot change instantaneously when struck by the TPA laser. However, the best SET response improvement is achieved in the current mirror with the internal negative feedback and capacitor combined together (solid red line in Fig. 21).

Next, the input transistor Q4 (one of the two input differential transistors) on the AC signal path is struck by the TPA laser, and the transient response at the non-inverting output terminal is measured. The measurement result in Fig. 7.22 shows that the internal negative feedback in the DC current mirror also improves the SET response in the AC signal path through the differential path (solid blue line in Fig. 7.22). However, the capacitor connected between the base of the reference device (Q1) and ground does not improve the SET response in the AC signal path (dotted magenta line in Fig. 22); there are not significant differences in the peak output transient of AC signal path with and without the capacitor as illustrated in Fig. 7.22 by the dotted black line (RE = 0 Ω and C = 0 F) and the dotted magenta line (RE = 0 Ω and C = 12 pF). The best SET response improvement in the AC signal path is achieved by the current mirror with the internal negative feedback and capacitor combined together (solid red line in Fig. 22).

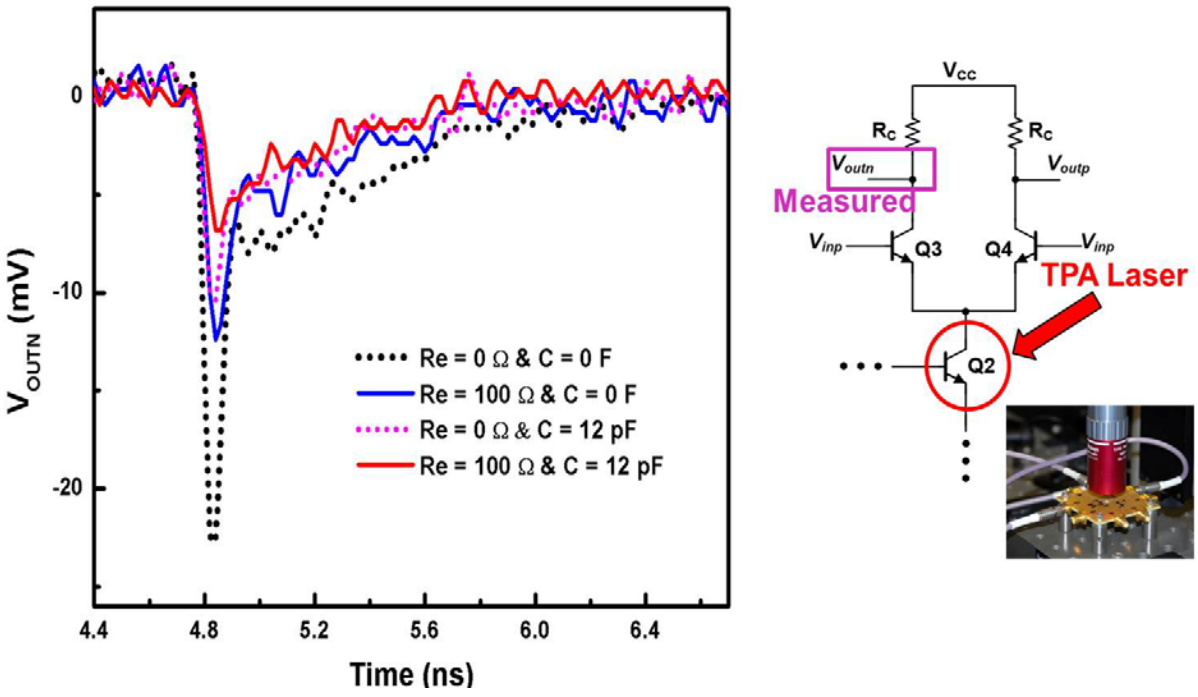


Fig. 7.21: Output device Q2 of the current mirrors is struck by the TPA laser, and the transient responses at the inverting output node are measured.

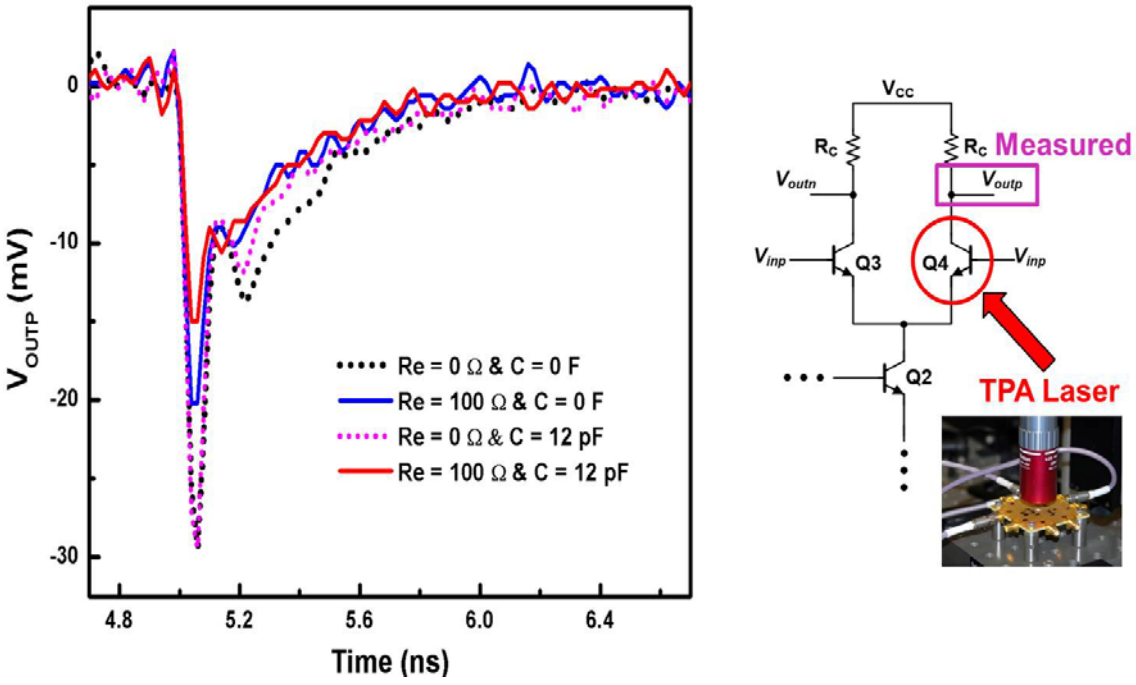


Fig. 7.22: Input transistor Q4 on the AC signal path is struck by the TPA laser, and the transient response at the non-inverting output terminal is measured.

7.6 Summary

This work has demonstrated how significantly a high-speed ADC can reduce the complexity of a receiver chain within a radar system as well as the time delay between the antenna and the baseband system enabling the radar system to operate in closer proximity to the true time domain. The radiation hardening technique utilizing an internal negative feedback from Chapter 6 is applied to the sub-analog components of the ADC to reduce single-event effects.

In addition, it has been demonstrated that the emitter degeneration resistor R_E (which creates internal negative feedback) in a DC current mirror improves the SET response not only in the output of the DC current mirror but also in the output of the AC signal path of the ECL circuit. Further improvement has been achieved together with a capacitor connected between the base of the reference device (Q1) and ground.

7.7 Acknowledgement

Seungwoo Jung would like to thank the Georgia Tech Research Institute (GTRI) and IBM for their support.

CHAPTER 8

CONCLUSION

This dissertation has presented how to utilize SiGe HBT BiCMOS technologies and employ radiation-hardening-by-design techniques in order to mitigate single-event effects in microelectronic circuits. It has been demonstrated in this work that both internal and external negative feedback schemes can significantly reduce the peak transient and settling time of the output signal during an ion strike; hence a circuit disturbed by a single-event transient can recover its original quiescent state (DC bias state) rapidly with negative feedback. Additionally, this work demonstrates the favorable characteristics of SiGe HBT BiCMOS technologies for use in a variety of applications through several studies, such as excellent linearity performance in the weakly-saturated SiGe HBTs investigation for low-power electronics, excellent noise performance in the C-SiGe LDO voltage regulator design, and excellent high-frequency performance in the DC-to-12 GHz input high-speed ADC design. Finally, a methodology to increase the bandwidth of a transimpedance amplifier for optical communication without compromising the gain is suggested.

The research discussed here has enabled the development of extreme-environment electronics such as a radiation hardened high-speed analog to digital converter (ADC) for the receiver and digital to analog converter (DAC) for the transmitter chain of radar systems.

8.1 Future Work

There are several extensions of this research.

1. Investigation of negative feedback effects on total-ionizing-dose (TID) damage.
2. Study of negative feedback effects in more complicated circuits such as operational amplifiers (op-amps).
3. Quantization of single-event effects based on various amount of feedback of a circuit
4. Applying weakly-saturated SiGe HBTs to low-power electronics and investigating single-event effects on them.
5. Investigation of low-frequency noise performance of complementary SiGe HBT LDO regulator at various ambient temperatures.

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